16 K-Channel Digital Switch with High Jitter Tolerance, Per Stream Rate Conversion (2, 4, 8, 16, or 32 Mbps), and 64 Inputs and 64 Outputs

Data Sheet

February 2006

Features

- 16,384-channel x 16,384-channel non-blocking unidirectional switching.The Backplane and Local inputs and outputs can be combined to form a non-blocking switching matrix with 64 input streams and 64 output streams
- 8,192-channel x 8,192-channel non-blocking Backplane input to Local output stream switch
- 8,192-channel x 8,192-channel non-blocking Local input to Backplane output stream switch
- 8,192-channel x 8,192-channel non-blocking Backplane input to Backplane output switch
- 8,192-channel x 8,192-channel non-blocking Local input to Local output stream switch
- Rate conversion on all data paths, Backplane-to-Local, Local-to-Backplane, Backplane-to-Backplane and Local-to-Local streams
- Backplane port accepts 32 input and 32 output ST-BUS streams with data rates of 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps in any combination, or a fixed allocation of 16 input and 16 output streams at 32.768 Mbps
- Local port accepts 32 input and 32 output ST-BUS streams with data rates of 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps in any combination, or a fixed allocation of 16 input and 16 output streams at 32.768 Mbps
- Exceptional input clock jitter tolerance (17 ns for 16 Mbps or lower data rates, 14 ns for 32 Mbps)
- Per-stream channel and bit delay for Local and Backplane input streams
- Per-stream advancement for Local and Backplane output streams
- Constant 2-frame throughput delay for frame integrity
- Per-channel high impedance output control for Local and Backplane streams

Ordering Information

ZL50060GAC	256 Ball PBGA	Trays
ZL50060GAG2	256 Ball PBGA**	Trays
ZL50061GAG	272 Ball PBGA	Trays
ZL50061GAG2	272 Ball PBGA**	Trays

**Pb Free Tin/Silver/Copper

-40°C to +85°C

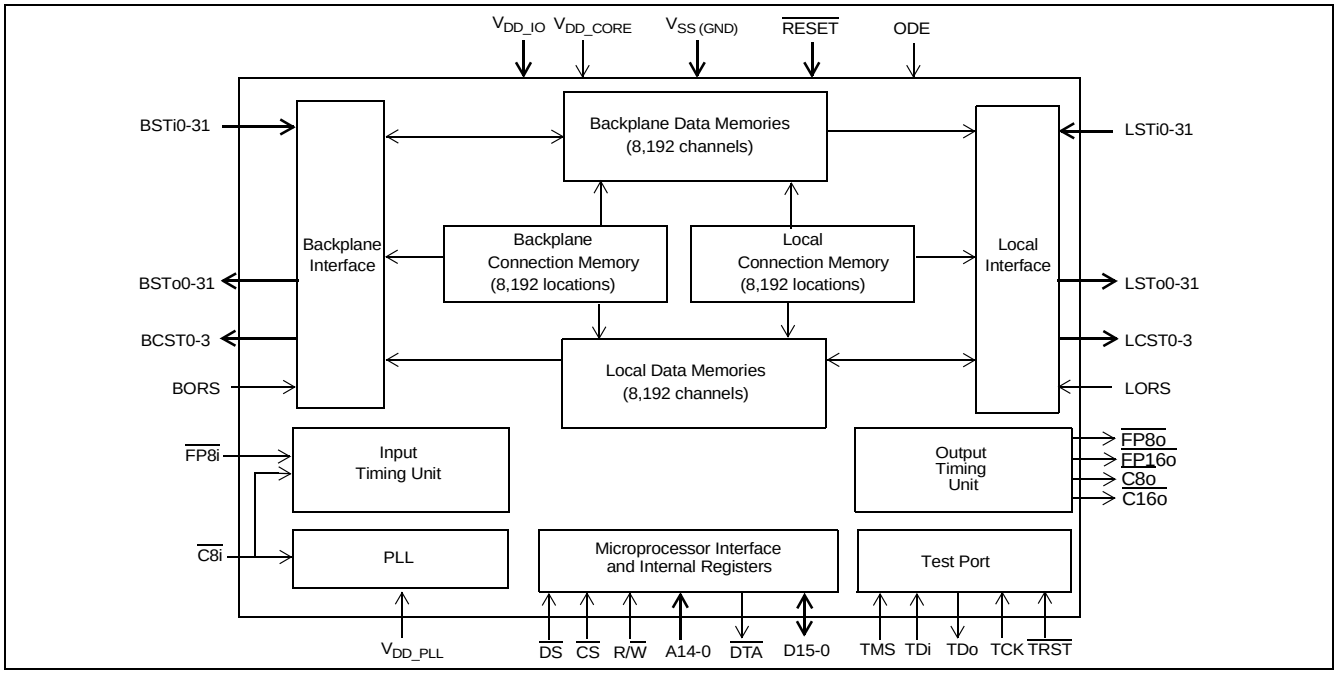

Figure 1 - ZL50060/1 Functional Block Diagram

- Per-channel driven-high output control for Local and Backplane streams
- High impedance control outputs for external drivers on Local and Backplane ports
- Per-channel message mode for Local and Backplane output streams
- Connection memory block programming for fast device initialization
- BER testing for Local and Backplane ports
- Automatic selection between ST-BUS and GCI-Bus operation
- Non-multiplexed Motorola microprocessor interface
- Conforms to the mandatory requirements of the IEEE-1149.1 (JTAG) standard
- Memory Built-In-Self-Test (BIST), controlled via microprocessor register
- 1.8 V core supply voltage
- 3.3 V I/O supply voltage
- 5 V tolerant inputs, outputs and I/Os
- ZL50061 is pin-to-pin compatible with Zarlink's MT90869 device [1]

Note 1: For software compatibility between ZL50061 and MT90869, please refer to Section 2.6.

Applications

- Central Office Switches (Class 5)
- Media Gateways
- Class-independent switches
- Access Concentrators
- Scalable TDM-Based Architectures
- Digital Loop Carriers

Device Overview

The ZL50060 and ZL50061 are two different packages of the same device. The ZL50060/1 has two data ports, the Backplane and the Local port. Both the Backplane and Local ports have two independent modes of operation, either 32 input and 32 output streams operated at 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps, in any combination, or 16 input and 16 output streams operated at 32.768 Mbps.

The ZL50060/1 contains two data memory blocks (Backplane and Local) to provide the following switching path configurations:

- Input-to-Output Unidirectional, supporting 16 K x 16 K switching
- Backplane-to-Local Bi-directional, supporting 8 K x 8 K data switching,
- Local-to-Backplane Bi-directional, supporting 8 K x 8 K data switching,
- Backplane-to-Backplane Bi-directional, supporting 8 K x 8 K data switching.
- Local-to-Local Bi-directional, supporting 8 K x 8 K data switching.

The device contains two connection memory blocks, one for the Backplane output and one for the Local output. Data to be output on the serial streams may come from either of the data memories (Connection Mode) or directly from the connection memory contents (Message Mode).

In Connection Mode, the contents of the connection memory define, for each output stream and channel, the source stream and channel (stored in data memory) to be switched.

In Message Mode, microprocessor data can be written to the connection memory for broadcast on the output streams on a per channel basis. This feature is useful for transferring control and status information to external circuits or other ST-BUS devices.

The device uses a master frame pulse ($\overline{\text{FP8i}}$) and master clock ($\overline{\text{C8i}}$) to define the input frame boundary and timing for both the Backplane port and the Local port. The device will automatically detect whether an ST-BUS or a GCI-Bus style frame pulse is being used. There is a two-frame delay from the time $\overline{\text{RESET}}$ is de-asserted to the establishment of full switch functionality. During this period, the input frame pulse format is determined before switching begins.

The device provides $\overline{\text{FP8o}}$, $\overline{\text{FP16o}}$, $\overline{\text{C8o}}$ and $\overline{\text{C16o}}$ outputs to support external devices connected to the outputs of the Backplane and Local ports.

A non-multiplexed Motorola microprocessor port allows programming of the various device operation modes and switching configurations. The microprocessor port provides access for Register read/write, Connection Memory read/write and Data Memory read-only operations. The port has a 15-bit address bus, 16-bit data bus and 4 control signals. The microprocessor may monitor channel data in the Backplane and Local data memories.

The mandatory requirements of the IEEE-1149.1 (JTAG) standard are fully supported via a dedicated test port.

The ZL50060 and ZL50061 are each available in one package:

- ZL50060: a 17 mm x 17 mm body, 1 mm ball-pitch, 256-PBGA.
- ZL50061: a 27 mm x 27 mm body, 1.27 mm ball-pitch, 272-PBGA.

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A1 corner identified by metallized marking

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GND	IC_GND	BSTo5	BSTo4	BSTo2	A2	VDD_CORE	A8	A11	A14	$\overline{DS}$	ODE	$\overline{DTA}$	TCK	BCSTo1	LCSTo3	LSTo0	LSTo1	LSTo2	NC
B	BSTo6	BSTo7	BSTo8	VDD_CORE	BSTo1	NC	A5	A7	A10	NC	$\overline{CS}$	VDD_CORE	TDi	$\overline{TRST}$	BCSTo2	LCSTo2	IC_GND	LSTo3	LSTo4	LSTo5
C	BSTo9	BSTo10	IC_GND	BSTo3	BSTo0	A1	A4	A6	NC	A13	R/$\overline{W}$	$\overline{RESET}$	TDo	BCSTo0	BCSTo3	LCSTo1	LCSTo0	LSTo6	LSTo7	LSTo8
D	BSTo11	BSTo12	BSTo13	GND	A0	VDD_IO	A3	GND	A9	A12	VDD_IO	TMS	GND	VDD_CORE	VDD_IO	IC_GND	GND	LSTo9	LSTo10	LSTo11
E	BSTo14	BSTo15	BSTo16	BSTo17													LSTo12	LSTo13	LSTo14	LSTo15
F	BSTo18	BSTo19	BSTo20	VDD_IO													VDD_IO	LSTo16	LSTo17	LSTo18
G	BSTo21	BSTo22	BSTo23	BSTo24													LSTo19	LSTo20	LSTo21	LSTo22
H	BSTo25	BSTo26	BSTo27	GND													GND	LSTo23	LSTo24	LSTo25
J	BSTo28	BSTo29	BSTo30	BSTo31					GND	GND	GND	GND					LSTo26	LSTo27	LSTo28	LSTo29
K	VDD_CORE	BORS	BSTi0	VDD_IO					GND	GND	GND	GND					LSTo30	LSTo31	LORS	VDD_CORE
L	BSTi1	BSTi2	BSTi3	BSTi4					GND	GND	GND	GND					VDD_IO	LSTi0	LSTi1	LSTi2
M	BSTi5	BSTi6	BSTi7	BSTi8					GND	GND	GND	GND					LSTi3	LSTi4	LSTi5	LSTi6
N	BSTi9	BSTi10	VDD_CORE	GND													GND	LSTi7	LSTi8	LSTi9
P	BSTi11	BSTi12	BSTi13	BSTi14													LSTi10	VDD_CORE	LSTi11	LSTi12
R	BSTi15	BSTI16	BSTi17	VDD_IO													VDD_IO	LSTi13	LSTi14	LSTi15
T	BSTi18	BSTi19	BSTi20	BSTi21													VDD_CORE	LSTi16	LSTi17	LSTi18
U	BSTi22	NC	NC	GND	BSTi28	VDD_IO	D10	GND	D4	VDD_IO	GND	VDD_PLL	GND	$\overline{FP8i}$	VDD_IO	VDD_CORE	GND	LSTi19	LSTi20	LSTi21
V	VDD_CORE	NC	NC	BSTi29	VDD_CORE	D13	D9	D7	D3	D0	IC_GND	NC	$\overline{C8o}$	$\overline{FP8o}$	NC	NC	LSTi22	LSTi23	LSTi24	LSTi25
W	BSTi23	BSTi24	BSTi25	BSTi30	D15	D12	D8	D6	D2	IC_GND	IC_GND	$\overline{C8i}$	$\overline{C16o}$	$\overline{FP16o}$	NC	NC	NC	LSTi26	LSTi27	NC
Y	BSTi26	BSTi27	NC	BSTi31	D14	D11	VDD_CORE	D5	D1	IC_GND	VDD_CORE	IC_OPEN	IC_OPEN	VDD_CORE	NC	NC	LSTi29	LSTi30	LSTi31	LSTi28

Figure 2 - ZL50061 PBGA Connections (272 PBGA, 27 mm x 27 mm) Pin Diagram
(as viewed through top of package)

Pinout Diagram: (as viewed through top of package)

A1 corner identified by metallized marking

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	A0	A1	A2	A3	A4	$\overline{DS}$	R/$\overline{W}$	$\overline{CS}$	BCSTo0	BCSTo1	BCSTo2	BCSTo3	LCSTo3	LCSTo2	LCSTo1	LCSTo0
B	BSTo0	BSTo1	BSTo2	BSTo3	A5	A6	A7	A8	A9	ODE	$\overline{RESET}$	TMS	LSTo0	LSTo1	LSTo2	LSTo3
C	BSTo4	BSTo5	BSTo6	BSTo7	A10	A11	A12	A13	A14	$\overline{DTA}$	TDi	TDo	LSTo4	LSTo5	LSTo6	LSTo7
D	BSTo8	BSTo9	BSTo10	BSTo11	BORS	IC_GND	IC_GND	IC_GND	IC_GND	TCK	$\overline{TRST}$	LORS	LSTo8	LSTo9	LSTo10	LSTo11
E	BSTo12	BSTo13	BSTo14	BSTo15	VDD_IO	VDD_IO	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_IO	VDD_IO	LSTo12	LSTo13	LSTo14	LSTo15
F	BSTo16	BSTo17	BSTo18	BSTo19	VDD_IO	VDD_CORE	GND	GND	GND	GND	VDD_CORE	VDD_IO	LSTo16	LSTo17	LSTo18	LSTo19
G	BSTo20	BSTo21	BSTo22	BSTo23	VDD_IO	GND	GND	GND	GND	GND	GND	VDD_IO	LSTo20	LSTo21	LSTo22	LSTo23
H	BSTo24	BSTo25	BSTo26	BSTo27	VDD_IO	GND	GND	GND	GND	GND	GND	VDD_IO	LSTo24	LST25	LSTo26	LSTo27
J	BSTo28	BSTo29	BSTo30	BSTo31	VDD_CORE	GND	GND	GND	GND	GND	GND	VDD_CORE	LSTo28	LSTo29	LSTo30	LSTo31
K	BSTi0	BSTi1	BSTi2	BSTi3	VDD_CORE	GND	GND	GND	GND	GND	GND	VDD_CORE	LSTi0	LSTi1	LSTi2	LSTi3
L	BSTi4	BSTi5	BSTi6	BSTi7	VDD_IO	VDD_CORE	VDD_CORE	GND	GND	VDD_CORE	VDD_CORE	VDD_IO	LSTi4	LSTi5	LSTi6	LSTi7
M	BSTi8	BSTi9	BSTi10	BSTi11	VDD_IO	D3	D2	D1	D0	VDD_PLL	NC	VDD_IO	LSTi8	LSTi9	LSTi10	LSTi11
N	BSTi12	BSTi13	BSTi14	BSTi15	BSTi16	D7	D6	D5	D4	IC_OPEN	IC_OPEN	LSTi12	LSTi13	LSTi14	LSTi15	LSTi16
P	BSTi17	BSTi18	BSTi19	BSTi20	BSTi21	D11	D10	D9	D8	$\overline{C16o}$	$\overline{FP16o}$	LSTi17	LSTi18	LSTi19	LSTi20	LSTi21
R	BSTi22	BSTi23	BSTi24	BSTi25	BSTi26	D15	D14	D13	D12	$\overline{FP8o}$	$\overline{FP8i}$	LSTi22	LSTi23	LSTi24	LSTi25	LSTi26
T	BSTi27	BSTi28	BSTi29	BSTi30	BSTi31	IC_GND	IC_GND	IC_GND	IC_GND	$\overline{C8i}$	$\overline{C8o}$	LSTi27	LSTi28	LSTi29	LSTi30	LSTi31

Figure 3 - ZL50060 PBGA Connections (256 PBGA, 17 mm x 17 mm) Pin Diagram
(as viewed through top of package)

Pin Description

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
Device Timing			
$\overline{C8i}$	W12	T10	**Master Clock (5 V Tolerant Schmitt-Triggered Input).** This pin accepts an 8.192 MHz clock. The internal frame boundary is aligned with the clock falling or rising edge, as controlled by the C8IPOL bit in the Control Register. Input data on both the Backplane and Local sides (BSTi0-31 and LSTi0-31) must be aligned to this clock and the accompanying input frame pulse, FP8i.
$\overline{FP8i}$	U14	R11	**Frame Pulse Input (5 V Tolerant Schmitt-Triggered Input)**. When the Frame Pulse Width bit (FPW) of the Control Register is LOW (default), this pin accepts a 122 ns-wide frame pulse. When the FPW bit is HIGH, this pin accepts a 244 ns-wide frame pulse. The device will automatically detect whether an ST-BUS or GCI-Bus style frame pulse is applied. Input data on both the Backplane and Local sides (BSTi0-31 and LSTi0-31) must be aligned to this frame pulse and the accompanying input clock, $\overline{C8i}$.
$\overline{C8o}$	V13	T11	**$\overline{C8o}$ Output Clock (5 V Tolerant Three-state Output).** This pin outputs an 8.192 MHz clock generated within the device. The clock falling edge or rising edge is aligned with the output frame boundary presented on FP8o; this edge polarity alignment is controlled by the COPOL bit of the Control Register. Output data on both the Backplane and Local sides (BSTo0-31 and LSTo0-31) will be aligned to this clock and the accompanying output frame pulse, $\overline{FP8o}$.
$\overline{FP8o}$	V14	R10	**Frame Pulse Output (5 V Tolerant Three-state Output).** When the Frame Pulse Width bit (FPW) of the Control Register is LOW (default), this pin outputs a 122 ns-wide frame pulse. When the FPW bit is HIGH, this pin outputs a 244 ns-wide frame pulse. The frame pulse, running at 8 kHz rate, will have the same format (ST-BUS or GCI-Bus) as the input frame pulse ($\overline{FP8i}$). Output data on both the Backplane and Local sides (BSTo0-31 and LSTo0-31) will be aligned to this frame pulse and the accompanying output clock, $\overline{C8o}$.
$\overline{C16o}$	W13	P10	**$\overline{C16o}$ Output Clock (5 V Tolerant Three-state Output).** This pin outputs a 16.384 MHz clock generated within the device. The clock falling edge or rising edge is aligned with the output frame boundary presented on FP16o; this edge polarity alignment is controlled by the COPOL bit of the Control Register. Output data on both the Backplane and Local sides (BSTo0-31 and LSTo0-31) will be aligned to this clock and the accompanying output frame pulse, $\overline{FP16o}$.

Pin Description (continued)

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
$\overline{\text{FP16o}}$	W14	P11	**Frame Pulse Output (5 V Tolerant Three-state Output).** When the Frame Pulse Width bit (FPW) of the Control Register is LOW (default), this pin outputs a 61 ns-wide frame pulse. When the FPW bit is HIGH, this pin outputs a 122 ns-wide frame pulse. The frame pulse, running at 8 kHz rate, will have the same format (ST-BUS or GCI-Bus) as the input frame pulse ($\overline{\text{FP8i}}$). Output data on both the Backplane and Local sides (BSTo0-31 and LSTo0-31) will be aligned to this frame pulse and the accompanying output clock, C16o.
Backplane and Local Inputs			
BSTi0-15	K3, L1, L2, L3, L4, M1, M2, M3, M4, N1, N2, P1, P2, P3, P4, R1	K1, K2, K3, K4, L1, L2, L3, L4, M1, M2, M3, M4, N1, N2, N3, N4	**Backplane Serial Input Streams 0 to 15 (5 V Tolerant Inputs with Internal Pull-downs).** In Backplane Non-32 Mbps Mode, these pins accept serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each input stream. In Backplane 32 Mbps Mode, these pins accept serial TDM data streams at a fixed data rate of 32.768 Mbps (with 512 channels per stream).
BSTi16-31	R2, R3, T1, T2, T3, T4, U1, W1, W2, W3, Y1, Y2, U5, V4, W4, Y4	N5, P1, P2, P3, P4, P5, R1, R2, R3, R4, R5, T1, T2, T3, T4, T5	**Backplane Serial Input Streams 16 to 31 (5 V Tolerant Inputs with Internal Pull-downs).** In Backplane Non-32 Mbps Mode, these pins accept serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each input stream. In Backplane 32 Mbps Mode, these pins are unused and should be externally connected to a defined logic level.

Pin Description (continued)

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
LSTi0-15	L18, L19, L20, M17, M18, M19, M20, N18, N19, N20, P17, P19, P20, R18, R19, R20	K13, K14, K15, K16, L13, L14, L15, L16, M13, M14, M15, M16, N12, N13, N14, N15	**Local Serial Input Streams 0 to 15 (5 V Tolerant Inputs with Internal Pull-downs).** In Local Non-32 Mbps Mode, these pins accept serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each input stream. In Local 32 Mbps Mode, these pins accept serial TDM data streams at a fixed data rate of 32.768 Mbps (with 512 channels per stream).
LSTi16-31	T18, T19, T20, U18, U19, U20, V17, V18, V19, V20, W18, W19, Y20, Y17, Y18, Y19	N16, P12, P13, P14, P15, P16, R12, R13, R14, R15, R16, T12, T13, T14, T15, T16	**Local Serial Input Streams 16 to 31 (5 V Tolerant Inputs with Internal Pull-downs).** In Local Non-32 Mbps Mode, these pins accept serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each input stream. In Local 32 Mbps Mode, these pins are unused and should be externally connected to a defined logic level.
Backplane and Local Outputs and Control			
ODE	A12	B10	**Output Drive Enable (5 V Tolerant Input with Internal Pull-up)**. An asynchronous input providing Output Enable control to the BSTo0-31, LSTo0-31, BCSTo0-3, and LCSTo0-3 outputs. When LOW, the BSTo0-31 and LSTo0-31 outputs are driven HIGH or high impedance (dependent on the **BORS** and **LORS** pin settings respectively) and the outputs BCSTo0-3 and LCSTo0-3 are driven low. When HIGH, the outputs BSTo0-31, LSTo0-31, BCSTo0-3, and LCSTo0-3 are enabled.

Pin Description (continued)

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
BORS	K2	D5	**Backplane Output Reset State (5 V Tolerant Input with Internal Pull-down)**. When this input is LOW, the device will initialize with the BSTo0-31 outputs driven high, and the BCSTo0-3 outputs driven low. Following initialization, the Backplane stream outputs are always active and a high impedance state, if required on a per-channel basis, may be implemented with external buffers controlled by outputs BCSTo0-3. When this input is HIGH, the device will initialize with the BSTo0-31 outputs at high impedance and the BCSTo0-3 outputs driven low. Following initialization, the Backplane stream outputs may be set active or high impedance using the **ODE** pin or on a per-channel basis with the **BE** bit in the Backplane Connection Memory.
BSTo0-15	C5, B5, A5, C4, A4, A3, B1, B2, B3, C1, C2, D1, D2, D3, E1, E2	B1, B2, B3, B4, C1, C2, C3, C4, D1, D2, D3, D4, E1, E2, E3, E4	**Backplane Serial Output Streams 0 to 15 (5 V Tolerant, Three-state Outputs with Slew-Rate Control)**. In Backplane Non-32 Mbps Mode, these pins output serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each output stream. In Backplane 32 Mbps Mode, these pins output serial TDM data streams at a fixed data rate of 32.768 Mbps (with 512 channels per stream). Refer to the descriptions of the **BORS** and **ODE** pins for control of the output HIGH or high impedance state.

Pin Description (continued)

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
BSTo16-31	E3, E4, F1, F2, F3, G1, G2, G3, G4, H1, H2, H3, J1, J2, J3, J4	F1, F2, F3, F4, G1, G2, G3, G4, H1, H2, H3, H4, J1, J2, J3, J4	**Backplane Serial Output Streams 16 to 31 (5 V Tolerant, Three-state Outputs with Slew-Rate Control).** In Backplane Non-32 Mbps Mode, these pins output serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each output stream. These pins are unused when the Backplane 32 Mbps Mode is selected. Therefore, the value output on these pins during Backplane 32 Mbps Mode (either driven-HIGH or high impedance) is dependent on the configuration of the BORS pin. Refer to the descriptions of the **BORS** and **ODE** pins for control of the output HIGH or high impedance state.
BCSTo0-3	C14, A15, B15, C15	A9, A10, A11, A12	**Backplane Output Channel high impedance Control (5 V Tolerant, Three-state Outputs).** These pins control external buffering individually for a set of Backplane output streams on a per-channel basis. When LOW, the external output buffer will be tri-stated. When HIGH, the external output buffer will be enabled. In Backplane Non-32 Mbps Mode (stream rates 2 Mbps to 16Mbps): BCSTo0 is the output enable for BSTo0,4,8,12,16,20,24,28 BCSTo1 is the output enable for BSTo1,5,9,13,17,21,25,29 BCSTo2 is the output enable for BSTo2,6,10,14,18,22,26,30 BCSTo3 is the output enable for BSTo3,7,11,15,19,23,27,31. In Backplane 32Mbps Mode (stream rate 32Mbps): BCSTo0 is the output enable for BSTo0,4,8,12 BCSTo1 is the output enable for BSTo1,5,9,13 BCSTo2 is the output enable for BSTo2,6,10,14 BCSTo3 is the output enable for BSTo3,7,11,15. Refer to the descriptions of the **BORS** and **ODE** pins for control of the output LOW or active state.

Pin Description (continued)

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
LORS	K19	D12	**Local Output Reset State (5 V Tolerant Input with Internal Pull-down)**. When this input is LOW, the device will initialize with the LSTo0-31 outputs driven high, and the LCSTo0-3 outputs driven low. Following initialization, the Local stream outputs are always active and a high impedance state, if required on a per-channel basis, may be implemented with external buffers controlled by outputs LCSTo0-3. When this input is HIGH, the device will initialize with the LSTo0-31 outputs at high impedance and the LCSTo0-3 outputs driven low. Following initialization, the Local stream outputs may be set active or high impedance using the **ODE** pin or on a per-channel basis with the **LE** bit in the Local Connection Memory.
LSTo0-15	A17, A18, A19, B18, B19, B20, C18, C19, C20, D18, D19, D20, E17, E18, E19, E20	B13, B14, B15, B16, C13, C14, C15, C16, D13, D14, D15, D16, E13, E14, E15, E16	**Local Serial Output Streams 0 to 15 (5 V Tolerant Three-state Outputs with Slew-Rate Control)**. In Local Non-32 Mbps Mode, these pins output serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each output stream. In Local 32 Mbps Mode, these pins output serial TDM data streams at a fixed data rate of 32.768 Mbps (with 512 channels per stream). Refer to the descriptions of the **LORS** and **ODE** pins for control of the output HIGH or high impedance state.

Pin Description (continued)

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
LSTo16-31	F18, F19, F20, G17, G18, G19, G20, H18, H19, H20, J17, J18, J19, J20, K17, K18	F13, F14, F15, F16, G13, G14, G15, G16, H13, H14, H15, H16, J13, J14, J15, J16	**Local Serial Output Streams 16 to 31 (5 V Tolerant Three-state Outputs with Slew-Rate Control)**. In Local Non-32 Mbps Mode, these pins output serial TDM data streams at a data rate of: 16.384 Mbps (with 256 channels per stream), 8.192 Mbps (with 128 channels per stream), 4.096 Mbps (with 64 channels per stream) or 2.048 Mbps (with 32 channels per stream). The data rate is independently programmable for each output stream. These pins are unused when the Local 32 Mbps Mode is selected. Therefore, the value output on these pins during Local 32 Mbps Mode (either driven-HIGH or high impedance) is dependent on the configuration of the LORS pin. Refer to the descriptions of the **LORS** and **ODE** pins for control of the output HIGH or high impedance state.
LCSTo0-3	C17, C16, B16, A16	A16, A15, A14, A13	**Local Output Channel high impedance Control (5 V Tolerant Three-state Outputs).** These pins control external buffering individually for a set of Local output streams on a per-channel basis. When LOW, the external output buffer will be tri-stated. When HIGH, the external output buffer will be enabled. In Local Non-32 Mbps Mode (stream rate 2 Mbps to 16 Mbps): LCSTo0 is the output enable for LSTo0,4,8,12,16,20,24,28 LCSTo1 is the output enable for LSTo1,5,9,13,17,21,25,29 LCSTo2 is the output enable for LSTo2,6,10,14,18,22,26,30 LCSTo3 is the output enable for LSTo3,7,11,15,19,23,27,31. In Local 32 Mbps Mode (stream rate 32 Mbps): LCSTo0 is the output enable for LSTo0,4,8,12 LCSTo1 is the output enable for LSTo1,5,9,13 LCSTo2 is the output enable for LSTo2,6,10,14 LCSTo3 is the output enable for LSTo3,7,11,15. Refer to descriptions of the **LORS** and **ODE** pins for control of the output LOW or active state.

Pin Description (continued)

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
Microprocessor Port Signals			
A0 - A14	D5, C6, A6, D7, C7, B7, C8, B8, A8, D9, B9, A9, D10, C10, A10	A1, A2, A3, A4, A5, B5, B6, B7, B8, B9, C5, C6, C7, C8, C9	**Address 0 - 14 (5 V Tolerant Inputs).** These pins form the 15-bit address bus to the internal memories and registers. A0 = LSB
D0 - D15	V10, Y9, W9, V9, U9, Y8, W8, V8, W7, V7, U7, Y6, W6, V6, Y5, W5	M9, M8, M7, M6, N9, N8, N7, N6, P9, P8, P7, P6, R9, R8, R7, R6	**Data Bus 0 - 15 (5 V Tolerant Inputs/Outputs with Slew-Rate Control).** These pins form the 16-bit data bus of the microprocessor port. D0 = LSB
$\overline{CS}$	B11	A8	**Chip Select (5 V Tolerant Input).** Active LOW input used by the microprocessor to enable the microprocessor port access. **Note that a minimum of 30 ns must separate the de-assertion of DTA (to high) and the assertion of $\overline{CS}$ and/or $\overline{DS}$ to initiate the next access.**
$\overline{DS}$	A11	A6	**Data Strobe (5 V Tolerant Input).** This active LOW input works in conjunction with $\overline{CS}$ to enable the microprocessor port read and write operations. **Note that a minimum of 30 ns must separate the de-assertion of DTA (to high) and the assertion of CS and/or $\overline{DS}$ to initiate the next access.**
R/$\overline{W}$	C11	A7	**Read/$\overline{Write}$ (5 V Tolerant Input).** This input controls the direction of the data bus lines (D0-D15) during a microprocessor access.
$\overline{DTA}$	A13	C10	**Data Transfer Acknowledgment (5 V Tolerant Three-state Output).** This active LOW output indicates that a data bus transfer is complete. A pull-up resistor is required to hold a HIGH level. **Note that a minimum of 30 ns must separate the de-assertion of DTA (to high) and the assertion of CS and/or DS to initiate the next access.**

Pin Description (continued)

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
$\overline{\text{RESET}}$	C12	B11	**Device Reset (5 V Tolerant Input with Internal Pull-up).** This input (active LOW) asynchronously applies reset and synchronously releases reset to the device. In the reset state, the outputs LSTo0-31 and BSTo0-31 are set to a HIGH or high impedance state, depending on the state of the LORS and BORS external control pins, respectively. The assertion of $\overline{\text{RESET}}$ causes the LCSTo0-3 and BCSTo0-3 pins to be driven LOW (refer to Table 2). The assertion of this pin also clears the device registers and internal counters. **Refer to Section 8.3 on page 47 for the timing requirements regarding this reset signal**.
JTAG Control Signals			
TCK	A14	D10	**Test Clock (5 V Tolerant Input).** Provides the clock to the JTAG test logic.
TMS	D12	B12	**Test Mode Select (5 V Tolerant Input with Internal Pull-up)**. JTAG signal that controls the state transitions of the TAP controller.
TDi	B13	C11	**Test Serial Data In (5 V Tolerant Input with Internal Pull-up).** JTAG serial test instructions and data are shifted in on this pin.
TDo	C13	C12	**Test Serial Data Out (5 V Tolerant Three-state Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in a high impedance state when JTAG is not enabled.
$\overline{\text{TRST}}$	B14	D11	**Test Reset (5 V Tolerant Input with Internal Pull-up).** Asynchronously initializes the JTAG TAP controller to the Test-Logic-Reset state. This pin must be pulsed LOW during power-up for JTAG testing. This pin must be held LOW for normal functional operation of the device.
Power and Ground Pins			
V_{DD_IO}	D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15	E5, E6, E11, E12, F5, F12, G5, G12, H5, H12, L5, L12, M5, M12	**Power Supply for Periphery Circuits:** +3.3 V
V_{DD_CORE}	A7, B4, B12, D14, K1, K20, N3, P18, T17, U16, V1, V5, Y7, Y11, Y14	E7, E8, E9, E10, F6, F11, J5, J12, K5, K12, L6, L7, L10, L11	**Power Supply for Core Circuits:** +1.8 V

Pin Description (continued)

Pin Name	ZL50061 Package Coordinates (272-ball PBGA)	ZL50060 Package Coordinates (256-ball PBGA)	Description
V_{DD_PLL}	U12	M10	**Power Supply for Analog PLL:** +1.8 V
V_{SS} (GND)	A1, D4, D8, D13, D17, H4, H17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, N4, N17, U4, U8, U11, U13, U17	F7, F8, F9, F10, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L8, L9	Ground.
Unused Pins			
NC	A20, B6, B10, C9, U2, U3, V2, V3, V12, V15, V16, W15, W16, W17, W20, Y3, Y15, Y16	M11	**No Connects.** These pins are not used and can be tied HIGH, LOW, or left unconnected.
IC_OPEN	Y12, Y13	N10, N11	**Internal Connections - OPEN.** These pins must be left unconnected.
IC_GND	A2, B17, C3, D16, V11, W10, W11, Y10	D6, D7, D8, D9, T6, T7, T8, T9	**Internal Connections - GND.** These pins must be tied LOW.

1.0 Unidirectional and Bi-directional Switching Applications

The ZL50060/1 has a maximum capacity of 16,384 input channels and 16,384 output channels. This is calculated from the maximum number of streams and channels: 64 input streams (32 Backplane, 32 Local) at 16.384 Mbps and 64 output streams (32 Backplane, 32 Local) at 16.384 Mbps.

A typical mode of operation is to separate the input and output streams to form a unidirectional switch, as shown in Figure 4 below.

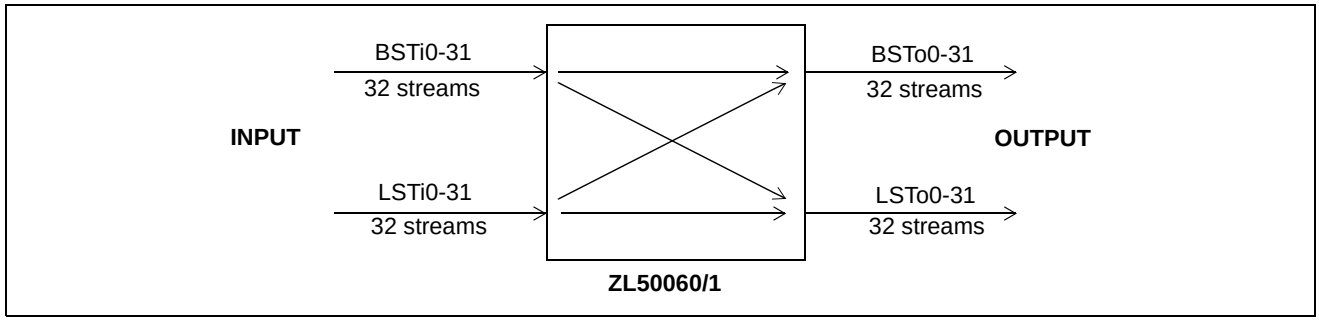


Figure 4 - 16,384 x 16,384 Channels (16 Mbps), Unidirectional Switching

In this system, the Backplane and Local input streams are combined, and the Backplane and Local output streams are combined, so that the switch appears as a 64 input stream by 64 output stream switch. This gives the maximum 16,384 x 16,384 channel capacity.

Often a system design needs to differentiate between a Backplane and a Local side, or it needs to put the switch in a bi-directional configuration. In this case, the ZL50060/1 can be used as shown in Figure 5 to give 8,192 x 8,192 channel bi-directional capacity.

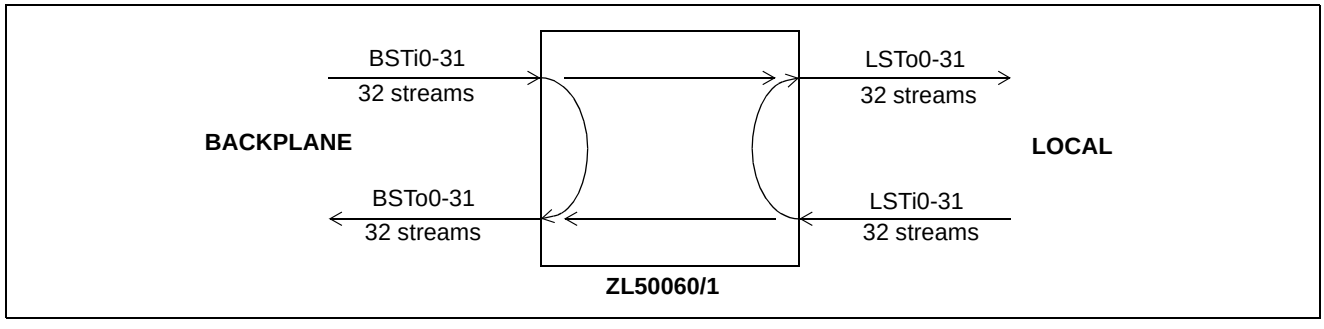


Figure 5 - 8,192 x 8,192 Channels (16 Mbps), Bi-directional Switching

In this system setup, the chip has a capacity of 8,192 input channels and 8,192 output channels on the Backplane side, as well as 8,192 input channels and 8,192 output channels on the Local side. Note that some or all of the output channels on one side can come from the other side, e.g., Backplane input to Local output switching.

Note that in either configuration, the Backplane port can be operated in the Backplane 32Mbps Mode, providing 512 channels on each of the 16 available input and output streams (BSTi0-15 and BSTo0-15) operating at a data rate of 32.768 Mbps, in conjunction with the Local streams (LSTi0-31 and LSTo0-31) operating at 16.384 Mbps (Local Non-32 Mbps Mode) or in conjunction with the Local streams (LSTi0-15 and LSTo0-15) operating at 32.768 Mbps (Local 32 Mbps Mode). Similarly, the Local port can be operated in the Local 32 Mbps Mode, providing 512 channels on each of the 16 available input and output streams (LSTi0-15 and LSTo0-15) operating at a data rate of 32.768 Mbps, in conjunction with the Backplane streams (BSTi0-31 and BSTo0-31) operating at 16.384 Mbps (Backplane Non-32 Mbps Mode) or in conjunction with the Backplane streams (BSTi0-15 and BSTo0-15) operating at 32.768 Mbps (Backplane 32 Mbps Mode).

The modes in which one port operates in 32Mbps Mode while the other port operates in Non-32 Mbps Mode allow data rate conversion between 32.768 Mbps and 16.384 Mbps without loss to the switching capacity.

1.1 Flexible Configuration

The ZL50060/1 can be configured as a 16 K by 16 K non-blocking unidirectional digital switch, an 8 K by 8 K non-blocking bi-directional digital switch, or as a blocking switch with various switching capacities.

1.1.1 Non-Blocking Unidirectional Configuration (Typical System Configuration)

Because the input and output drivers are synchronous, the user can combine input Backplane streams and input Local streams as well as output Backplane streams and output Local streams to increase the total number of input and output streams of the switch in a unidirectional configuration, as shown in Figure 4.

- 16,384-channel x 16,384-channel non-blocking switching from input to output streams

1.1.2 Non-Blocking Bi-directional Configuration

Another typical application is to configure the ZL50060/1 as a non-blocking 8 K by 8 K bi-directional switch, as shown in Figure 5:

- 8,192-channel x 8,192-channel non-blocking switching from Backplane input to Local output streams
- 8,192-channel x 8,192-channel non-blocking switching from Local input to Backplane output streams
- 8,192-channel x 8,192-channel non-blocking switching from Backplane input to Backplane output streams
- 8,192-channel x 8,192-channel non-blocking switching from Local input to Local output streams

1.1.3 Blocking Bi-directional Configuration

The ZL50060/1 can be configured as a blocking bi-directional switch if it is an application requirement. For example, it can be configured as a 12 K by 4 K bi-directional blocking switch, as shown in Figure 6:

- 12,288-channel x 4,096-channel blocking switching from Backplane input to Local output streams
- 4,096-channel x 12,288-channel blocking switching from Local input to Backplane output streams
- 12,288-channel x 12,288-channel non-blocking switching from Backplane input to Backplane output streams
- 4,096-channel x 4,096-channel non-blocking switching from Local input to Local output streams

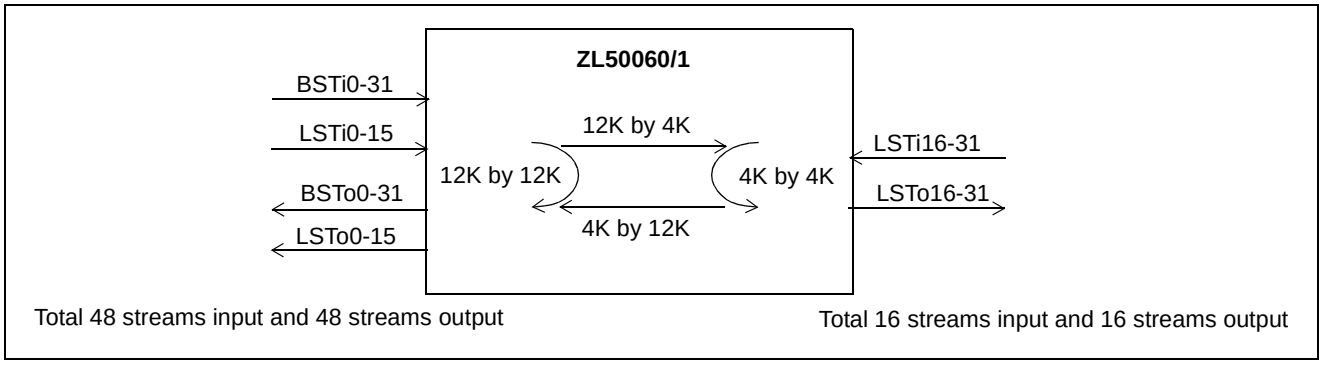


Figure 6 - 12,288 by 4,096 Channels Blocking Bi-directional Configuration

2.0 Functional Description

2.1 Switching Configuration

The device supports five switching configurations: (1) Unidirectional switch, (2) Backplane-to-Local, (3) Local-to-Backplane, (4) Backplane-to-Backplane, and (5) Local-to-Local. The following sections describe the switching paths in detail. Configurations (2) - (5) enable a non-blocking bi-directional switch with 8,192 Backplane input/output channels at Backplane stream data rates of 16.384 Mbps or 32.768 Mbps, and 8,192 Local input/output channels at Local stream data rates of 16.384 Mbps or 32.768 Mbps. The switching paths of configurations (2) to (5) may be operated simultaneously. When the lower data-rates of 8.192, 4.096 and 2.048 Mbps are included, there will be a corresponding reduction in switch capacity although conversion between differing rates will be maintained.

2.1.1 Unidirectional Switch

The device can be configured as a 16,384 x 16,384 unidirectional switch by grouping together all input streams and all output streams. All streams can be operated at a data rate of 16.384 Mbps or 32.768 Mbps, or a combination of 16.384 Mbps and 32.768 Mbps (i.e., one rate on the Local streams and the other rate on the Backplane streams). Lower data rates may be used with a corresponding reduction in switch capacity.

2.1.2 Backplane-to-Local Path

The device can provide data switching between the Backplane input port and the Local output port. The Local Connection Memory determines the switching configurations.

2.1.3 Local-to-Backplane Path

The device can provide data switching between the Local input port and the Backplane output port. The Backplane Connection Memory determines the switching configurations.

2.1.4 Backplane-to-Backplane Path

The device can provide data switching between the Backplane input and output ports. The Backplane Connection Memory determines the switching configurations.

2.1.5 Local-to-Local Path

The device can provide data switching between the Local input and output ports. The Local Connection Memory determines the switching configurations.

2.1.6 Port Data Rate Modes and Selection

The bit rate for each input stream is selected by writing to dedicated input bit rate registers, BIBRR0 to BIBRR31 for Backplane Input Bit Rate Registers (see Table 50) and LIBRR0 to LIBRR31 for Local Input Bit Rate Registers (see Table 46).

The bit rate for each output stream is selected by writing to dedicated output bit rate registers, BOBRR0 to BOBRR31 for Backplane Output Bit Rate Registers (see Table 52) and LOBRR0 to LOBRR31 for Local Output Bit Rate Registers (see Table 48).

If the Backplane 32 Mbps Mode is selected by setting the Control Register bit MODE32B HIGH, the settings in BIBRRn and BOBRRn are ignored. Similarly, if the Local 32 Mbps Mode is selected by setting the Control Register bit MODE32L HIGH, the settings in LIBRRn and LOBRRn are ignored.

Stream Numbers	Rate Selection Capability (for each individual stream)
Local Input streams - LSTi0-15	2.048, 4.096, 8.192 or 16.384 Mbps in Local Non-32 Mbps Mode. All streams at 32.768 Mbps in Local 32 Mbps Mode.
Local Input streams - LSTi16-31	2.048, 4.096, 8.192 or 16.384 Mbps in Local Non-32 Mbps Mode. Unused in Local 32 Mbps Mode.
Backplane Input streams - BSTi0-15	2.048, 4.096, 8.192 or 16.384 Mbps in Backplane Non-32 Mbps Mode. All streams at 32.768 Mbps in Backplane 32 Mbps Mode.
Backplane Input streams - BSTi16-31	2.048, 4.096, 8.192 or 16.384 Mbps in Backplane Non-32 Mbps Mode. Unused in Backplane 32 Mbps Mode.
Local Output streams - LSTo0-15	2.048, 4.096, 8.192 or 16.384 Mbps in Local Non-32 Mbps Mode. All streams at 32.768 Mbps in Local 32 Mbps Mode.
Local Output streams - LSTo16-31	2.048, 4.096, 8.192 or 16.384 Mbps in Local Non-32 Mbps Mode. Unused in Local 32 Mbps Mode.
Backplane Output streams - BSTo0-15	2.048, 4.096, 8.192 or 16.384 Mbps in Backplane Non-32 Mbps Mode. All streams at 32.768 Mbps in Backplane 32Mbps Mode.
Backplane Output streams - BSTo16-31	2.048, 4.096, 8.192 or 16.384 Mbps in Backplane Non-32 Mbps Mode. Unused in Backplane 32 Mbps Mode.

Table 1 - Per-stream Input and Output Data Rate Selection: Backplane and Local

2.1.7 Local Port Rate Selection

The Local port has 32 input (LSTi0-31) and 32 output (LSTo0-31) data streams.

The Local streams can be operated in one of two modes, Local Non-32 Mbps Mode and Local 32 Mbps Mode. The Local stream data rates are not affected by the operating mode of the Backplane port. The operating mode of the Local side is determined by the state of the Control Register bit MODE32L. Setting this bit HIGH will invoke the Local 32 Mbps Mode. Setting the bit LOW will invoke the Non-32 Mbps Mode. The default value of this bit on device reset is LOW. The timing of the input and output clocks and frame pulses is shown in Figure 8, “Input and Output Frame Pulse Alignment for Different Data Rates” on page 28.

Local Non-32 Mbps Mode: Each of the Local streams (LSTi0-31 and LSTo0-31) can be independently programmed for a data rate of 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps.

Local 32 Mbps Mode: 16 of the Local input streams (LSTi0-15) and 16 of the Local output streams (LSTo0-15) operate at a fixed rate of 32.768 Mbps. In this mode, the remaining input and output streams are unused.

2.1.7.1 Local Input Port

The input traffic on the Local streams are aligned based on the $\overline{\text{FP8i}}$ and $\overline{\text{C8i}}$ input timing signals. Each input stream, LSTi0-31, can be individually set to operate at 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps by programming the LIBR1-0 bits in the Local Input Bit Rate Register (LIBRR0-31). The Local streams can also be set to operate at 32.768 Mbps. When the MODE32L bit in the Control Register is set high, the first 16 input streams, LSTi0-15, operate at 32.768 Mbps and the remaining 16 streams, LSTi16-31, will not be used and must be connected to a defined logic level.

2.1.7.2 Local Output Port

The output traffic on the Local streams are aligned based on the $\overline{\text{FP8o}}$ and $\overline{\text{C8o}}$ output timing signals. Operation of stream data in Connection Mode or Message Mode is determined by the state of the LMM bit of the Local Connection Memory. The channel high impedance state is controlled by the LE bit of the Local Connection Memory. The data source (i.e. from the Local or Backplane Data Memory) is determined by the LSRC bit of the Local Connection Memory. Refer to Section 9.1, Local Connection Memory, and Section 12.3, Local Connection Memory Bit Definition for more details. Each output stream, LSTo0-31, can be individually set to operate at 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps by programming the LOBR1-0 bits in the Local Output Bit Rate Register (LOBRR0-31). The Local streams can also be set to operate at 32.768 Mbps. When the MODE32L bit in the Control Register is set high, the first 16 output streams, LSTo0-15, operate at 32.768 Mbps and the remaining 16 streams, LSTo16-31, will not be used and must be connected to a defined logic level.

2.1.8 Backplane Port Rate Selection

The Backplane port has 32 input (BSTi0-31) and 32 output (BSTo0-31) data streams.

The Backplane streams can be operated in one of two modes, Backplane Non-32 Mbps Mode and Backplane 32 Mbps Mode. The Backplane stream data rates are not affected by the operating mode of the Local port. The operating mode of the Backplane side is determined by the state of the Control Register bit MODE32B. Setting this bit HIGH will invoke the Backplane 32 Mbps Mode. Setting the bit LOW will invoke the Non-32 Mbps Mode. The default value of this bit on device reset is LOW. The timing of the input and output clocks and frame pulses is shown in Figure 8, “Input and Output Frame Pulse Alignment for Different Data Rates” on page 28.

Backplane Non-32 Mbps Mode: Each of the Backplane streams (BSTi0-31 and BSTo0-31) can be independently programmed for a data rate of 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps.

Backplane 32 Mbps Mode: 16 of the Backplane input streams (BSTi0-15) and 16 of the Backplane output streams (BSTo0-15) operate at a fixed rate of 32.768 Mbps. In this mode, the remaining input and output streams are unused.

2.1.8.1 Backplane Input Port

The input traffic on the Backplane streams are aligned based on the $\overline{\text{FP8i}}$ and $\overline{\text{C8i}}$ input timing signals. Each input stream, BSTi0-31, can be individually set to operate at 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps by programming the BIBR1-0 bits in the Backplane Input Bit Rate Register (BIBRR0-31). The Backplane streams can also be set to operate at 32.768 Mbps. When the MODE32B bit in the Control Register is set high, the first 16 input streams, BSTi0-15, operate at 32.768 Mbps and the remaining 16 streams, BSTi16-31, will not be used and must be connected to a defined logic level.

2.1.8.2 Backplane Output Port

The output traffic on the Backplane streams are aligned based on the $\overline{\text{FP8o}}$ and $\overline{\text{C8o}}$ output timing signals. Operation of stream data in Connection Mode or Message Mode is determined by the state of the BMM bit of the Backplane Connection Memory and the channel high impedance state is controlled by the BE bit of the Backplane Connection Memory. The data source (i.e. from the Local or Backplane Data Memory) is determined by the BSRC bit of the Backplane Connection Memory. Refer to Section 9.2, Backplane Connection Memory and Section 12.4, Backplane Connection Memory Bit Definition for more details. Each output stream, BSTo0-31, can be individually set to operate at 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps by programming the BOBR1-0 bits in the Backplane Output Bit Rate Register (BOBRR0-31). The Backplane streams can also be set to operate at 32.768 Mbps. When the MODE32B bit in the Control Register is set high, the first 16 output streams, BSTo0-15, operate at 32.768 Mbps and the remaining 16 streams, BSTo16-31, will not be used and must be connected to a defined logic level.

2.2 Frame Pulse Input and Master Input Clock Timing

The input frame pulse ($\overline{FP8i}$) is an 8 kHz input signal active for 122 ns or 244 ns at the frame boundary. The FPW bit in the Control Register must be set according to the applied pulse width. See Pin Description and Table 19, “Control Register Bits” on page 56, for details.

The active state and timing of $\overline{FP8i}$ can conform either to the ST-BUS or to the GCI-Bus as shown in Figure 7, ST-BUS and GCI-Bus Input Timing Diagram for Different Data Rates. The ZL50060/1 device will automatically detect whether an ST-BUS or a GCI-Bus style frame pulse is being used for the master frame pulse ($\overline{FP8i}$). The output frame pulses ($\overline{FP8o}$ and $\overline{FP16o}$) are always of the same style (ST-BUS or GCI-Bus) as the input frame pulse. The active edge of the input clock ($\overline{C8i}$) shall be selected by the state of the Control Register bit C8IPOL.

Note that the active edge of ST-BUS is falling edge, which is the default mode of the device, while GCI-Bus uses rising edge as the active edge. Although GCI frame pulse will be automatically detected, to fully conform to GCI-Bus operation, the device should be set to use $\overline{C8i}$ rising edge as the active edge (by setting bit C8IPOL HIGH) when GCI-Bus is used.

For the purposes of describing the device operation, the remaining part of this document assumes the ST-BUS frame pulse format with a single width frame pulse of 122ns and a falling active clock-edge, unless explicitly stated otherwise.

In addition, the device provides $\overline{FP8o}$, $\overline{FP16o}$, $\overline{C8o}$ and $\overline{C16o}$ outputs to support external devices which connect to the output ports. The generated frame pulses ($\overline{FP8o}$, $\overline{FP16o}$) will be provided in the same format as the master frame pulse ($\overline{FP8i}$). The polarity of $\overline{C8o}$ and $\overline{C16o}$, at the frame boundary, can be controlled by the Control Register bit, COPOL. An analog phase lock loop (APLL) is used to multiply the input clock frequency on $\overline{C8i}$ to generate an internal clock signal operating at 131.072MHz.

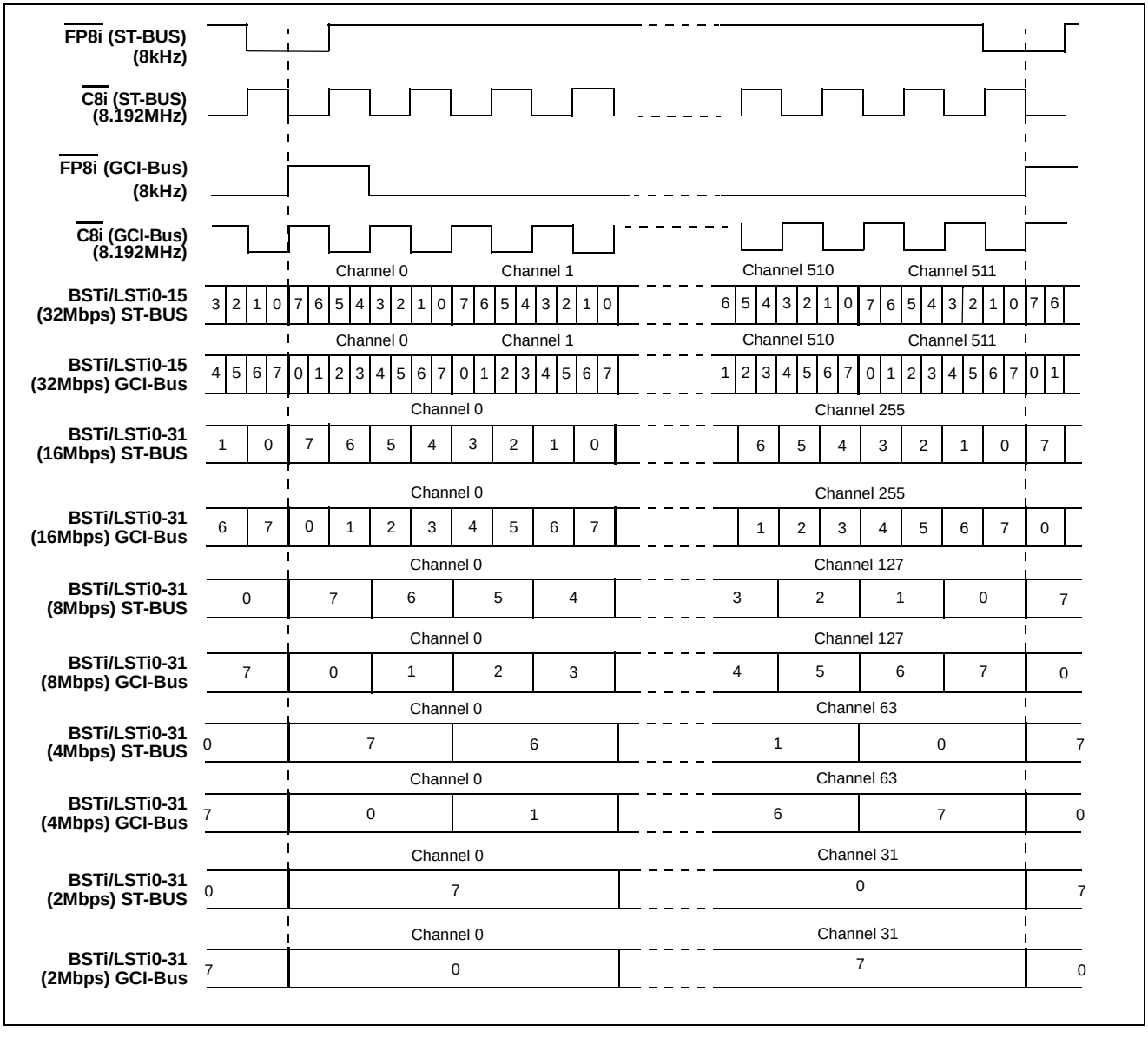


Figure 7 - ST-BUS and GCI-Bus Input Timing Diagram for Different Data Rates

2.3 Input Frame Pulse and Generated Frame Pulse Alignment

The ZL50060/1 accepts a frame pulse ($\overline{FP8i}$) and generates two frame pulse outputs, $\overline{FP8o}$ and $\overline{FP16o}$, which are aligned to the master frame pulse. There is a constant throughput delay for data being switched from the input to the output of the device such that data which is input during Frame N is output during Frame N+2.

For further details of frame pulse conditions and options, see Section 14.1, Control Register (CR), Figure 23, Frame Boundary Conditions, ST-BUS Operation, and Figure 24, Frame Boundary Conditions, GCI-Bus Operation.

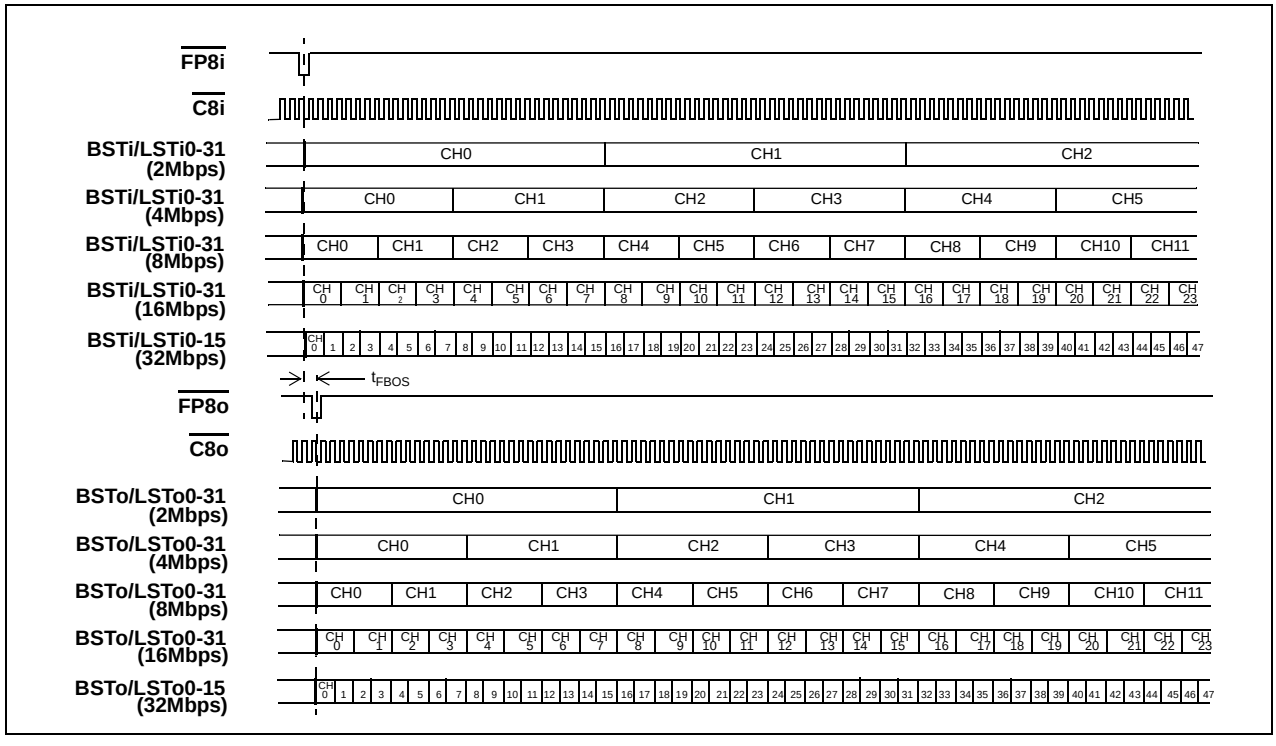


Figure 8 - Input and Output Frame Pulse Alignment for Different Data Rates

The t_{FBOS} is the offset between the input frame pulse, $\overline{FP8i}$, and the generated output frame pulse, $\overline{FP8o}$. Refer to the “AC Electrical Characteristics,” on page 83. Note that although the figure above shows the traditional setups of the frame pulses and clocks for both ST-BUS and GCI-Bus configurations, the devices can be configured to accept/generate double-width frame pulses (if the FPW bit in the Control Register is set) as well as to use the opposite clock edge for frame-boundary determination (using the C8IPOL and COPOL bits in the Control Register). See the timing diagrams in “AC Electrical Characteristics,” on page 83 for all of the available configurations.

2.4 Jitter Tolerance Improvement Circuit - Frame Boundary Discriminator

To improve the jitter tolerance of the ZL50060/1, a Frame Boundary Discriminator (FBD) circuit was added to the device. This circuit is enabled by setting the Control Register bit FBDEN to HIGH. By default the FBD is disabled.

The FBD can operate in two modes, as controlled by the FBD_MODE[2:0] bits of the Control Register. When bits FBD_MODE[2:0] are set to 000_B, the FBD is set to handle lower frequency jitter only (<8kHz). When bits FBD_MODE[2:0] are set to 111_B, the FBD can handle both low frequency and high frequency jitter. All other values are reserved. These bits are ignored when bit FBDEN is LOW. It is strongly recommended that if bit FBDEN is set HIGH, bits FBD_MODE[2:0] should be set to 111_B to improve the high frequency jitter handling capability.

To achieve the best jitter tolerance performance, it is also recommended that the input data sampling point be optimized. In most applications, the optimum sampling point is 1/2 instead of the default 3/4 (it can be changed by programming all the LIDR and BIDR registers). This will give more allowance for sampling point variations caused

by jitter. There are, however, some cases where data experience more delay than the timing signals. A common example is when multiple data lines are tied together to form bidirectional buses. The large bus loading may cause data to be delayed. If this is the case, the optimum sampling point may be 3/4 or 4/4 instead of 1/2. The optimum sampling point is dependent on the application. The user should optimize the sampling point to achieve the best jitter tolerance performance.

2.5 Input Clock Jitter Tolerance

Input clock jitter tolerance depends on the data rate. In general, the higher the data rate, the smaller the jitter tolerance is, because the period of a bit cell is shorter, and the sampling point variation allowance is smaller.

Jitter tolerance can not be accurately represented by just one number. Jitter of the same amplitude but different frequency spectrum can have different effect on the operation of a device. For example, a device that can tolerate 20 ns of jitter of 10 kHz frequency may only be able to tolerate 10 ns of jitter of 1 MHz frequency. Therefore, jitter tolerance should be represented as a spectrum over frequency. The highest possible jitter frequency is half of the carrier frequency. In the case of the ZL50060/1, the input clock is 8.192 MHz, and the jitter associated with this clock can have the highest frequency component at 4.096 MHz.

For the above reasons, jitter tolerance of the ZL50060/1 has been characterized at two data rates, 16.384 Mbps and 32.768 Mbps. The lower data rates (2.048 Mbps, 4.096 Mbps, 8.192 Mbps) will have the same or better tolerance than that of the 16.384 Mbps operation. Tolerance of jitter of different frequencies are shown in the “AC Electrical Characteristics“ section, table “Input Clock Jitter Tolerance“ on page 93. The Jitter Tolerance Improvement Circuit was enabled (Control Register, bit FBDEN set HIGH, and bits FBD_MODE[2:0] set to 111_B), and the sampling point was optimized.

2.6 Backward Compatibility with MT90869

The ZL50061 is pin-to-pin compatible with Zarlink’s MT90869 device. To ensure software compatibility between the two devices, the user must consider the following items:

1. The ZL50061 has enhanced input clock jitter tolerance. To maximize the jitter tolerance, the Frame Boundary Discriminator (FBD) circuit has to be enabled by setting bits FBDEN and FBD_MODE[2:0] in the Control Register HIGH. In MT90869, these bits are un-used. The input data sampling point also needs to be optimized by programming all the LIDR and BIDR registers. These are described in details in Section 2.4.
2. When Bit Error Rate (BER) transmission is enabled, all the channels on all same side (Local/Backplane) as the target BER transmission channel(s) will be unable to switch traffic. Also, the BER Counters (LBCR and BBCR) will not rollover. They will saturate when they reach their maximum value. These are described in more details in Section 6.0.
3. The hardware reset signal ($\overline{\text{RESET}}$) must be de-asserted less than 12 µs after the frame boundary or more than 13 µs after the frame boundary, as described in Section 8.3. This can be achieved, for example, by synchronizing the de-assertion of the reset signal with the input frame pulse.

3.0 Input and Output Offset Programming

Various registers are used to control the input sampling point (delay) and the output advancement for the Local and Backplane streams. The following sections explain the details of these offset programming features.

3.1 Input Offsets

Control of the Input Channel Delay and the Input Bit Delay allows each input stream to have a different frame boundary with respect to the master frame pulse, $\overline{\text{FP8i}}$.

The use of Input Channel Delay in combination with Input Bit Delay enables the Ch0 position to be placed anywhere within a frame to a resolution of 1/4 of the bit period.

3.1.1 Input Channel Delay Programming (Backplane and Local Input Streams)

By programming the Backplane or Local Input Channel Delay Registers (BCDR0 - BCDR31 and LCDR0 - LCDR31), users can individually assign the Ch0 position of each input stream to be located at any Of the channel boundaries in a frame. For delays within channel boundaries, the input bit delay programming can be used.

By default, all input streams have a channel delay of zero such that Ch0 is the first channel that appears after the frame boundary.

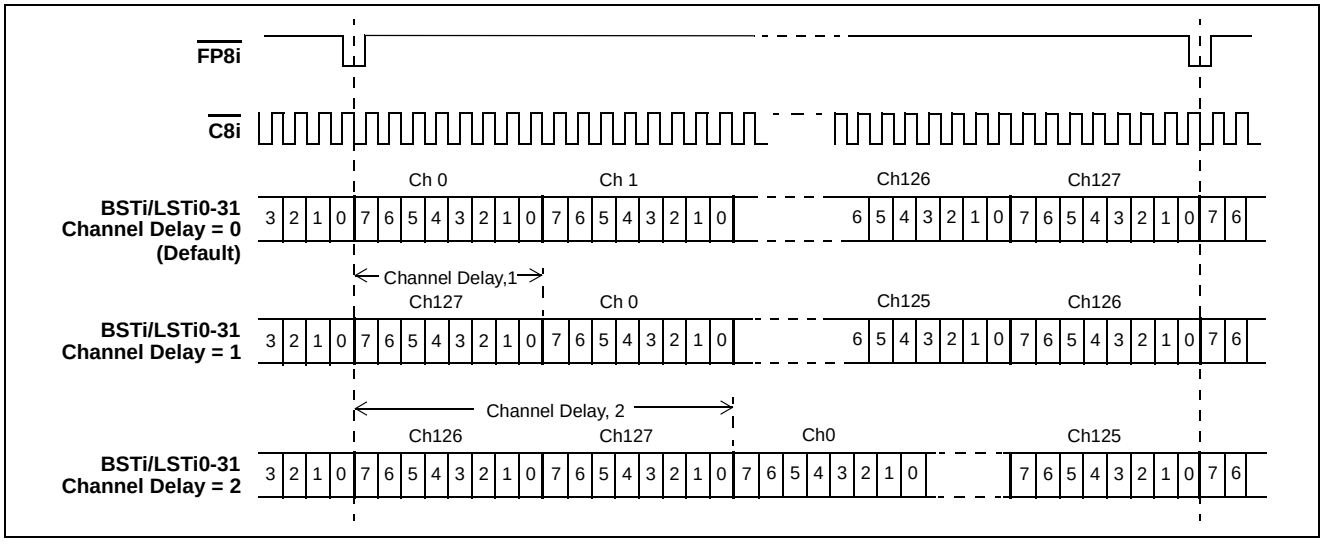


Figure 9 - Backplane and Local Input Channel Delay Timing Diagram (assuming 8 Mbps operation)

3.1.2 Input Bit Delay Programming (Backplane and Local Input Streams)

In addition to the Input Channel Delay programming, Input Bit Delay Registers LIDR0-31 and BIDR0-31 work in conjunction with the SMPL_MODE bit in the Control Register to allow users to control input bit fractional delay as well as input bit sample point selection for greater flexibility when designing switch matrices for high speed operation.

When SMPL_MODE = LOW (input bit fractional delay mode), bits LID[4:0] and BID[4:0] in the LIDR0-31 and BIDR0-31 registers respectively define the input bit fractional delay of the corresponding local and backplane stream. The total delay can be up to 7 3/4 bits with a resolution of 1/4 bit at the selected data rate. When SMPL_MODE = HIGH (sampling point select mode), bits LID[1:0] and BID[1:0] define the input bit sampling point of the stream. The sampling point can be programmed at the 3/4, 4/4, 1/4 or 2/4 bit location to allow better tolerance for input jitter. Bits LID[4:2] and BID[4:2] define the integer input bit delay, with a maximum value of 7 bits at a resolution of 1 bit.

Refer to Figure 10 and Figure 11 for Input Bit Delay Timing at 16 Mbps and 8 Mbps data rates, respectively.

Refer to Figure 11 for Input Sampling Point Selection Timing at 8 Mbps data rates.

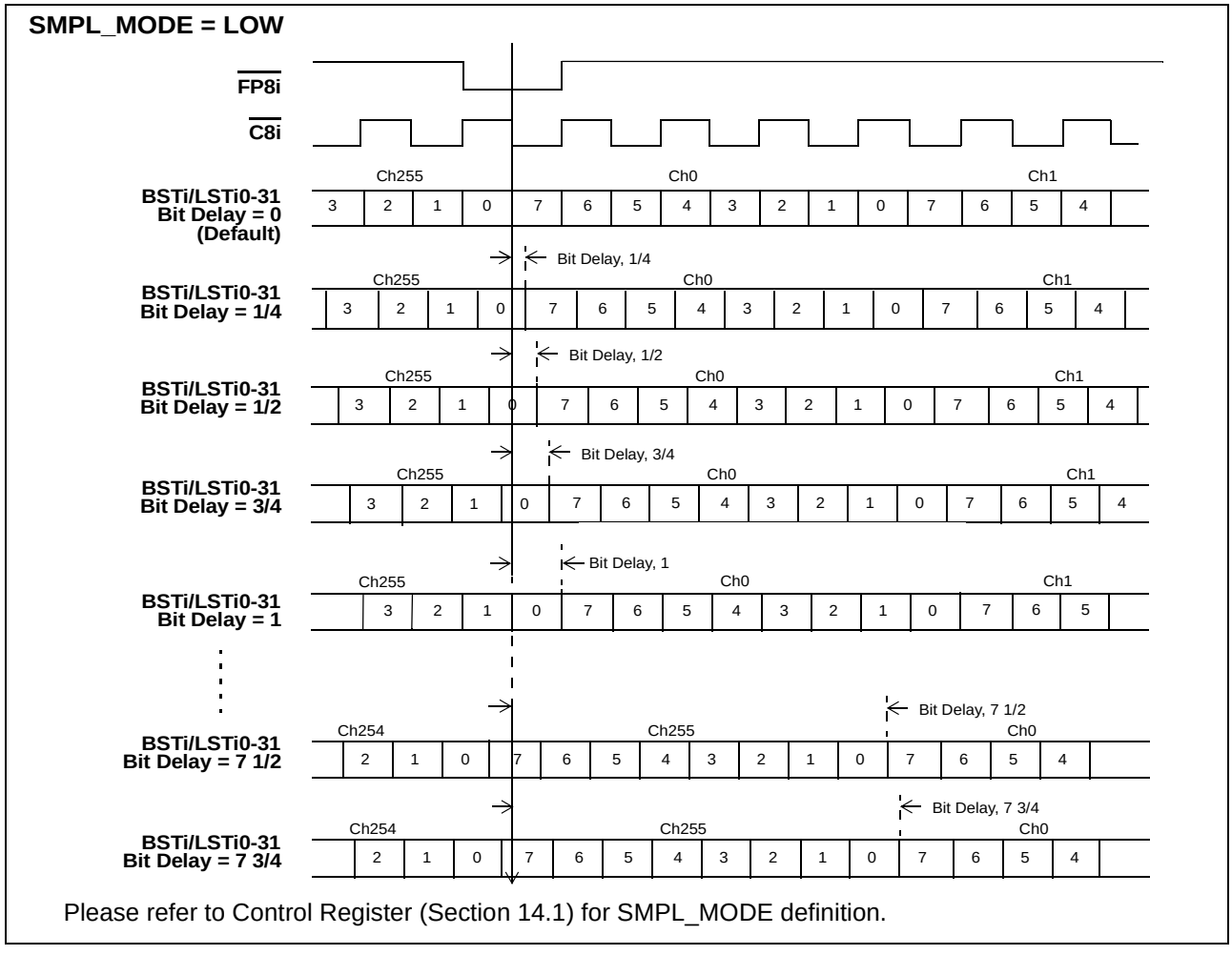


Figure 10 - Backplane and Local Input Bit Delay Timing Diagram for Data Rate of 16 Mbps

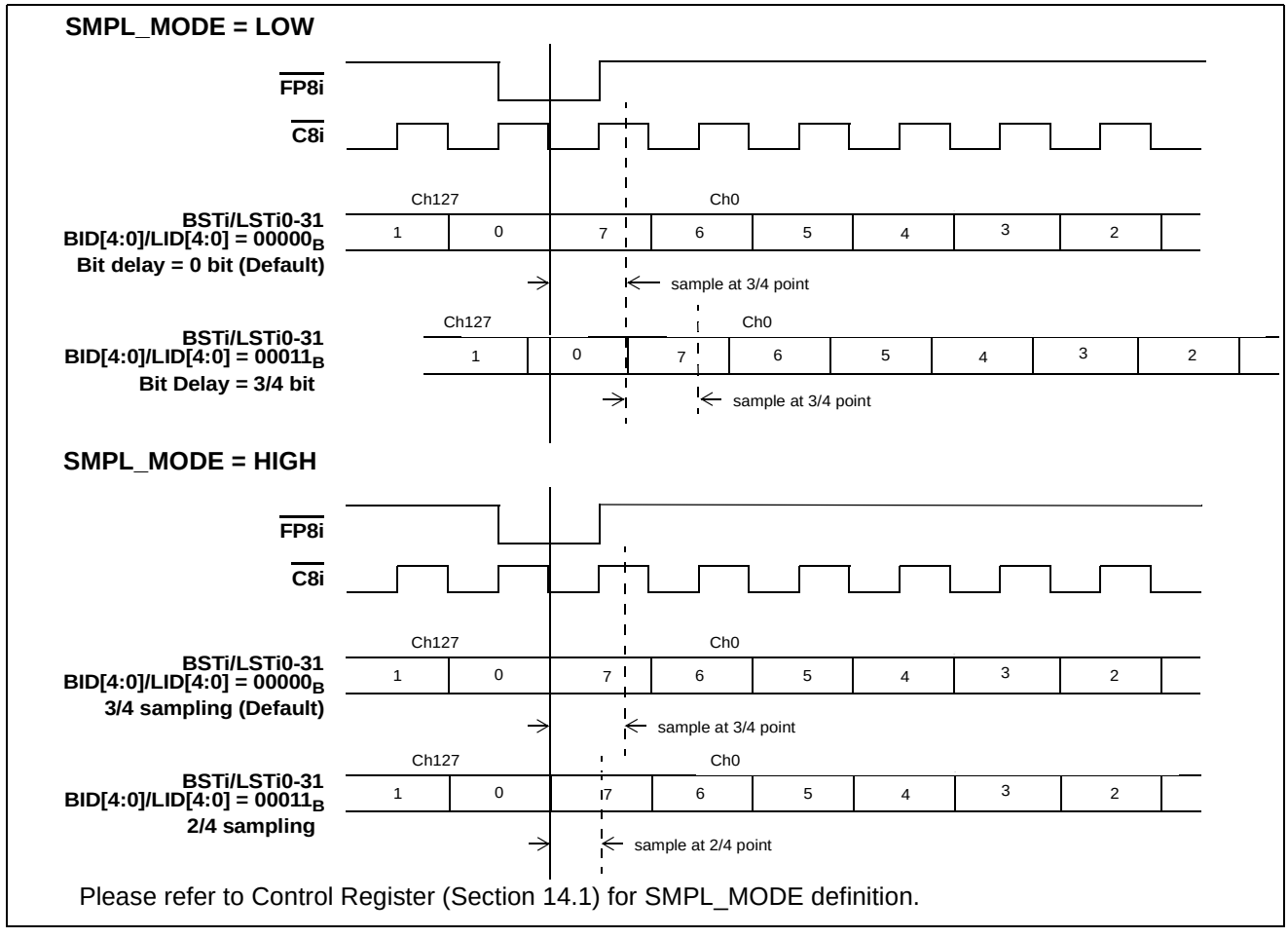


Figure 11 - Backplane and Local Input Bit Delay or Sampling Point Selection Timing Diagram for Data Rate of 8 Mbps

3.2 Output Advancement Programming (Backplane and Local Output Streams)

This feature is used to advance the output channel alignment of individual Local or Backplane output streams with respect to the frame boundary FP8o. Each output stream has its own advancement value that can be programmed by the Output Advancement Registers. The output advancement selection is useful in compensating for various parasitic loading on the serial data output pins.

The Local and Backplane Output Advancement Registers, LOAR0 - LOAR31 and BOAR0 - BOAR31, are used to control the Local and Backplane output advancement respectively. The advancement is determined with reference to the internal system clock rate (131.072 MHz). For 2 Mbps, 4 Mbps, 8 Mbps or 16 Mbps streams, the advancement can be 0, -2 cycles, -4 cycles or -6 cycles, which converts to approximately 0 ns, -15 ns, -31 ns or -46 ns as shown in Figure 12. For 32 Mbps streams, the advancement can be 0, -1 cycle, -2 cycles or -3 cycles, which converts to approximately 0ns, -7.6 ns, -15 ns or -23 ns.

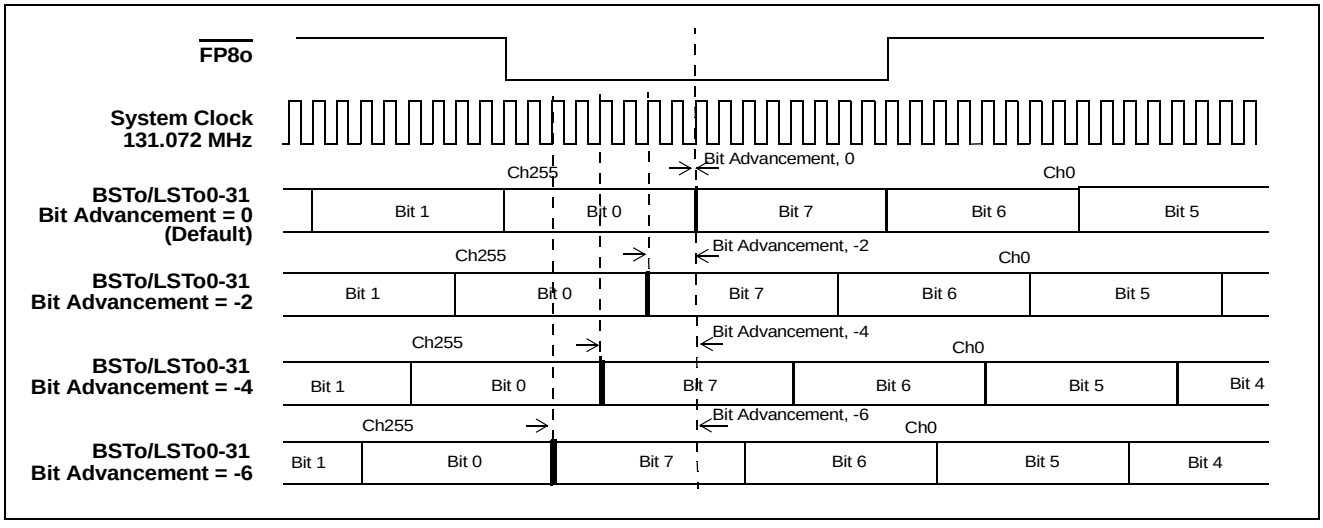


Figure 12 - Local and Backplane Output Advancement Timing Diagram for Data Rate of 16 Mbps

4.0 Port high impedance Control

The input pins, **LORS** and **BORS**, select whether the Local (**LSTo0-31**) and Backplane (**BSTo0-31**) output streams, respectively, are set to high impedance at the output of the device itself, or are always driven (active HIGH or active LOW). In the latter case (i.e., always driven), a high impedance state, if required on a per-channel basis, is invoked through an external interface circuit controlled by the **LCSTo0-3/BCSTo0-3** signals.

Setting **LORS/BORS** to a LOW state will configure the output streams, **LSTo0-31/BSTo0-31,** to transmit bi-state channel data with per-channel high impedance determined by external circuits under the control of the **LCSTo0-3/BCSTo0-3** outputs.

Setting **LORS/BORS** to a HIGH state will configure the output streams, **LSTo0-31/BSTo0-31,** of the device to invoke a high impedance output on a per-channel basis when required as controlled by the LE/BE bit.

The state of the **LORS/BORS** pin is detected and the device configured accordingly during a **$\overline{\text{RESET}}$** operation, e.g. following power-up. The **LORS/BORS** pin is an asynchronous input and is expected to be hard-wired for a particular system application, although it may be driven under logic control if preferred.

The Local/Backplane output enable control in order of highest priority is: $\overline{\text{RESET}}$, ODE, OSB, LE/BE.

$\overline{\text{RESET}}$ (input pin)	**ODE (input pin)**	**OSB (Control Register bit)**	**LE/BE (Local / Backplane Connection Memory bit)**	**LORS/BORS (input pin)**	**LSTo0-31/ BSTo0-31**	**LCSTo0-3/ BCSTo0-3**
0	X	X	X	0	HIGH	LOW
0	X	X	X	1	HI-Z	LOW
1	0	X	X	0	HIGH	LOW
1	0	X	X	1	HI-Z	LOW
1	1	0	X	0	HIGH	LOW
1	1	0	X	1	HI-Z	LOW
1	1	1	0	0	HIGH	LOW

Table 2 - Local and Backplane Output Enable Control Priority

$\overline{\text{RESET}}$ (input pin)	ODE (input pin)	OSB (Control Register bit)	LE/BE (Local / Backplane Connection Memory bit)	LORS/BORS (input pin)	LSTo0-31/ BSTo0-31	LCSTo0-3/ BCSTo0-3
1	1	1	0	1	HI-Z	LOW
1	1	1	1	X	ACTIVE (HIGH or LOW)	ACTIVE (HIGH or LOW)

Table 2 - Local and Backplane Output Enable Control Priority (continued)

4.1 LORS/BORS Asserted LOW, Non-32Mbps Mode

The data (channel control bit) transmitted by **L/BCSTo0-3** replicates the Local/Backplane Output Enable (**LE/BE**) bit of the Local/Backplane Connection Memory, with a LOW state indicating the channel to be set to high impedance. Refer to “Local Connection Memory Bit Definition,” on page 52 and “Backplane Connection Memory Bit Definition,” on page 53 for more details.

The **L/BCSTo0-3** pins transmit serial data (channel control bits) at 16.384 Mbps, with each bit representing the per-channel high impedance state for a specific stream. Eight output streams are allocated to each control line as follows:

- L/BCSTo0 outputs the channel control bits for streams L/BSTo0, 4, 8, 12, 16, 20, 24, and 28
- L/BCSTo1 outputs the channel control bits for streams L/BSTo1, 5, 9, 13, 17, 21, 25, and 29
- L/BCSTo2 outputs the channel control bits for streams L/BSTo2, 6, 10, 14, 18, 22, 26 and 30
- L/BCSTo3 outputs the channel control bits for streams L/BSTo3, 7, 11, 15, 19, 23, 27 and 31

The channel control bit location, within a frame period, for each channel of the Local/Backplane output streams is presented in Table 3, L/BCSTo Allocation of Channel Control Bits to Output Streams (Non-32 Mbps Mode).

As an aid to the description, the channel control bit for a single channel on specific streams is presented, with reference to Table 3:

1. The channel control bit corresponding to Stream 0, Channel 0, **L/BSTo0_Ch0,** is transmitted on **L/BCSTo0** and is advanced, relative to the frame boundary, by 10 periods of **C16o**.
2. The channel control bit corresponding to Stream 28, Channel 0, **L/BSTo28_Ch0,** is transmitted on **L/BCSTo0** in advance of the frame boundary by three periods of output clock, **C16o**. Similarly, the channel control bits for **L/BSTo29_Ch0**, **L/BSTo30_Ch0** and **L/BSTo31_Ch0** are advanced relative to the frame boundary by three periods of **C16o**, on **L/BCSTo1**, **L/BCSTo2** and **L/BCSTo3**, respectively.

The **L/BCSTo0-3** pins output data at a constant data rate of 16.384Mbps, independent of the data rate selected for the individual output streams, **L/BSTo0-31**. Streams at data rates lower than 16.384 Mbps will have the value of their respective channel control bit repeated for the duration of the channel. The bit will be repeated twice for 8.192 Mbps streams, four times for 4.096 Mbps streams and eight times for 2.048 Mbps streams. The channel control bit is not repeated for 16.384 Mbps streams.

Examples are presented, with reference to Table 3:

3. With stream **L/BSTo4** selected to operate at a data rate of 2.048Mbps, the value of the channel control bit for **Channel 0** will be transmitted during the **C16o** clock period numbers 2040, 2048, 8, 16, 24, 32, 40 and 48.
4. With stream **L/BSTo8** operated at a data rate of 8.192 Mbps, the value of the channel control bit for **Channel 1** will be transmitted during the **C16o** clock period numbers 9 and 17.

	Allocated Stream No.				Channel No. [2]				
C16o Period[1]	L/BCSTo0	L/BCSTo1	L/BCSTo2	L/BCSTo3	16 Mbps	8 Mbps	4 Mbps	2 Mbps	
2039	0 [3-1]	1	2	3	Ch 0	Ch 0	Ch 0	Ch 0	
2040	4 [3-3]	5	6	7	Ch 0	Ch 0	Ch 0	Ch 0	
2041	8	9	10	11	Ch 0	Ch 0	Ch 0	Ch 0	
2042	12	13	14	15	Ch 0	Ch 0	Ch 0	Ch 0	
2043	16	17	18	19	Ch 0	Ch 0	Ch 0	Ch 0	
2044	20	21	22	23	Ch 0	Ch 0	Ch 0	Ch 0	
2045	24	25	26	27	Ch 0	Ch 0	Ch 0	Ch 0	
2046	28 [3-2]	29 [3-2]	30 [3-2]	31 [3-2]	Ch 0	Ch 0	Ch 0	Ch 0	
2047	0	1	2	3	Ch 1	Ch 0	Ch 0	Ch 0	
2048	4 [3-3]	5	6	7	Ch 1	Ch 0	Ch 0	Ch 0	Frame
1	8	9	10	11	Ch 1	Ch 0	Ch 0	Ch 0	Boundary
2	12	13	14	15	Ch 1	Ch 0	Ch 0	Ch 0	
3	16	17	18	19	Ch 1	Ch 0	Ch 0	Ch 0	
4	20	21	22	23	Ch 1	Ch 0	Ch 0	Ch 0	
5	24	25	26	27	Ch 1	Ch 0	Ch 0	Ch 0	
6	28	29	30	31	Ch 1	Ch 0	Ch 0	Ch 0	
7	0	1	2	3	Ch 2	Ch 1	Ch 0	Ch 0	
8	4 [3-3]	5	6	7	Ch 2	Ch 1	Ch 0	Ch 0	
9	8 [3-4]	9	10	11	Ch 2	Ch 1	Ch 0	Ch 0	
10	12	13	14	15	Ch 2	Ch 1	Ch 0	Ch 0	
11	16	17	18	19	Ch 2	Ch 1	Ch 0	Ch 0	
12	20	21	22	23	Ch 2	Ch 1	Ch 0	Ch 0	
13	24	25	26	27	Ch 2	Ch 1	Ch 0	Ch 0	
14	28	29	30	31	Ch 2	Ch 1	Ch 0	Ch 0	
15	0	1	2	3	Ch 3	Ch 1	Ch 0	Ch 0	
16	4 [3-3]	5	6	7	Ch 3	Ch 1	Ch 0	Ch 0	
17	8 [3-4]	9	10	11	Ch 3	Ch 1	Ch 0	Ch 0	
etc.	etc.	etc.	etc.	etc.	etc.	etc.	etc.	etc.	
etc.	etc.	etc.	etc.	etc.	etc.	etc.	etc.	etc.	
2029	etc.	etc.	etc.	etc.	Ch 254	Ch 127	Ch 63	Ch 31	
2030	28	29	30	31	Ch 254	Ch 127	Ch 63	Ch 31	
2031	0	1	2	3	Ch 255	Ch 127	Ch 63	Ch 31	
2032	4	5	6	7	Ch 255	Ch 127	Ch 63	Ch 31	
2033	8	9	10	11	Ch 255	Ch 127	Ch 63	Ch 31	
2034	12	13	14	15	Ch 255	Ch 127	Ch 63	Ch 31	

Table 3 - L/BCSTo Allocation of Channel Control Bits to Output Streams (Non-32 Mbps Mode)

	Allocated Stream No.				Channel No. [2]				
C16o Period[1]	L/BCSTo0	L/BCSTo1	L/BCSTo2	L/BCSTo3	16 Mbps	8 Mbps	4 Mbps	2 Mbps	
2035	16	17	18	19	Ch 255	Ch 127	Ch 63	Ch 31	
2036	20	21	22	23	Ch 255	Ch 127	Ch 63	Ch 31	
2037	24	25	26	27	Ch 255	Ch 127	Ch 63	Ch 31	
2038	28	29	30	31	Ch 255	Ch 127	Ch 63	Ch 31	
2039	0 [3-1]	1	2	3	Ch 0	Ch 0	Ch 0	Ch 0	
2040	4 [3-3]	5	6	7	Ch 0	Ch 0	Ch 0	Ch 0	
2041	8	9	10	11	Ch 0	Ch 0	Ch 0	Ch 0	
2042	12	13	14	15	Ch 0	Ch 0	Ch 0	Ch 0	
2043	16	17	18	19	Ch 0	Ch 0	Ch 0	Ch 0	
2044	20	21	22	23	Ch 0	Ch 0	Ch 0	Ch 0	
2045	24	25	26	27	Ch 0	Ch 0	Ch 0	Ch 0	
2046	28 [3-2]	29 [3-2]	30 [3-2]	31 [3-2]	Ch 0	Ch 0	Ch 0	Ch 0	
2047	0	1	2	3	Ch 1	Ch 0	Ch 0	Ch 0	
2048	4 [3-3]	5	6	7	Ch 1	Ch 0	Ch 0	Ch 0	Frame
1	8	9	10	11	Ch 1	Ch 0	Ch 0	Ch 0	Boundary
2	12	13	14	15	Ch 1	Ch 0	Ch 0	Ch 0	
3	16	17	18	19	Ch 1	Ch 0	Ch 0	Ch 0	
etc.	etc.	etc.	etc.	etc.	etc.	etc.	etc.	etc.	

Table 3 - L/BCSTo Allocation of Channel Control Bits to Output Streams (Non-32 Mbps Mode) (continued)

Note 1: Clock period count is referenced to frame boundary.

Note 2: The channel numbers presented relate to the data rate selected for a specific stream.

Note 3: 3-1 to 3-4: See above for examples of channel control bits for streams of different data rates.

Figure 13, Local/Backplane Port External High Impedance Control Timing (Non-32 Mbps Mode) shows the channel control bits for **L/BCSTo0**, **L/BCSTo1**, **L/BCSTo2** and **L/BCSTo3** in one possible scenario which includes stream **L/BSTo0** at a data rate of 16.384 Mbps, **L/BSTo1** at 8.192 Mbps, **L/BSTo6** at 4.096 Mbps and **L/BSTo7** at 2.048 Mbps. All remaining streams are operated at a data rate of 16.384 Mbps.

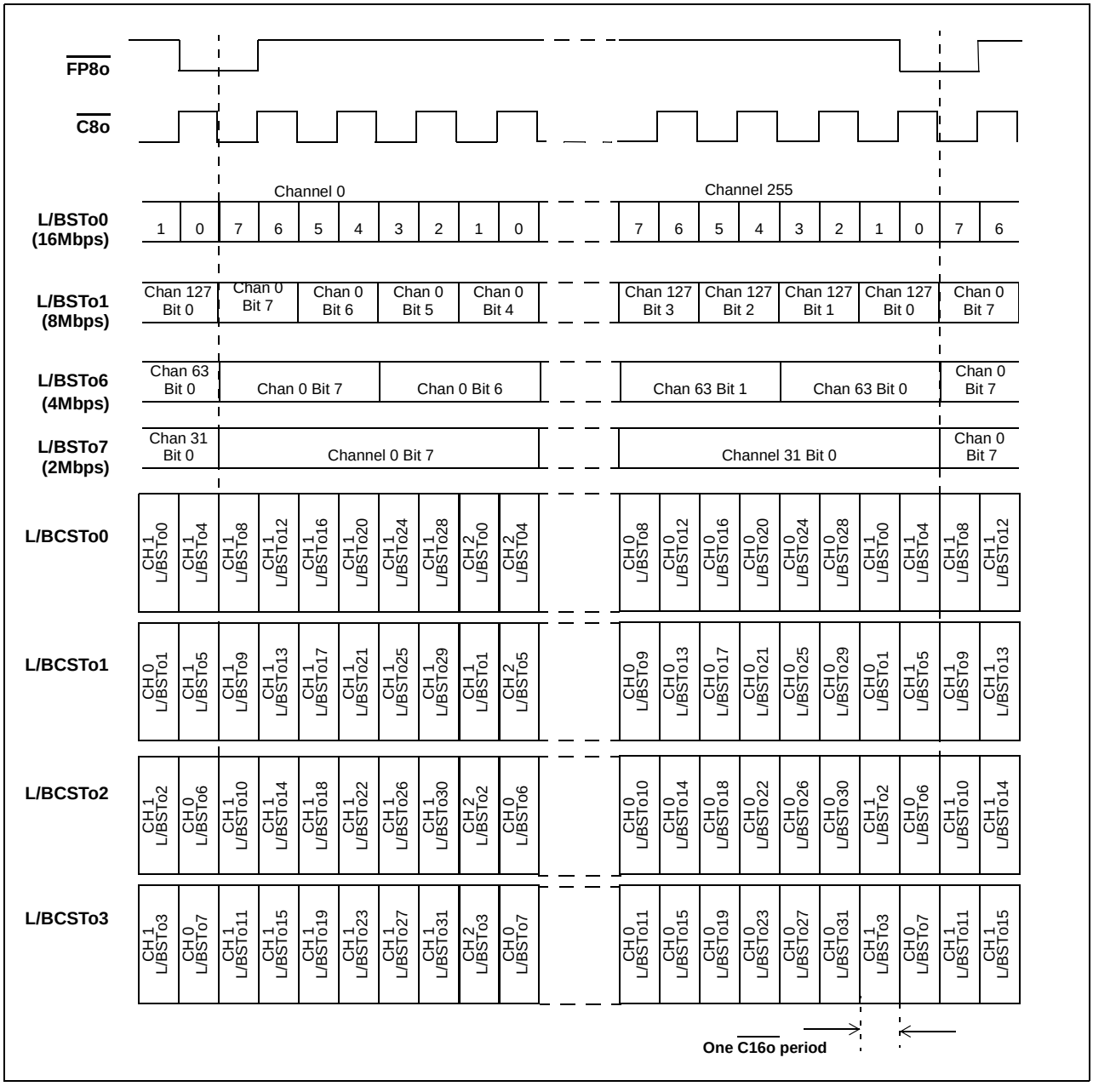


Figure 13 - Local/Backplane Port External High Impedance Control Timing (Non-32 Mbps Mode)

4.2 LORS/BORS Asserted LOW, 32Mbps Mode

Note that when the devices are operating in Local or Backplane 32 Mbps mode, some of the output streams (the upper half of the available streams) are unused. The LE/BE bits of the channels on those output streams will always be low. Therefore, the upper LSTo/BSTo pins are either driven HIGH or high impedance, in accordance with the value of the LORS/BORS input signals, as shown in Table 2 on page 33.

The data (channel control bit) transmitted by **L/BCSTo0-3** replicates the Local/Backplane Output Enable (**LE/BE**) bit of the Local/Backplane Connection Memory, with a LOW state indicating the channel to be set to high impedance. Refer to “Local Connection Memory Bit Definition,” on page 52 and “Backplane Connection Memory Bit Definition,” on page 53 for more details.

The **L/BCSTo0-3** pins transmit serial data (channel control bits) at 16.384 Mbps, with each bit representing the per-channel high impedance state for a specific stream. Four output streams are allocated to each control line as follows:

- L/BCSTo0 outputs the channel control bits for streams L/BSTo0, 4, 8, and 12
- L/BCSTo1 outputs the channel control bits for streams L/BSTo1, 5, 9, and 13
- L/BCSTo2 outputs the channel control bits for streams L/BSTo2, 6, 10, and 14
- L/BCSTo3 outputs the channel control bits for streams L/BSTo3, 7, 11, and 15

The channel control bit location, within a frame period, for each channel of the Local/Backplane output streams is presented in Table 4, L/BCSTo Allocation of Channel Control Bits to Output Streams (32 Mbps Mode)

The **L/BCSTo0-3** pins output data at a constant data rate of 16.384 Mbps and all output streams, **L/BSTo0-15**, operate at a data rate of 32.768 Mbps.

As an aid to the description, the channel control bit for a single channel on specific streams is presented, with reference to Table 4:

1. The channel control bit corresponding to Stream 0, Channel 0, **L/BSTo0_Ch0,** is transmitted on **L/BCSTo0** and is advanced, relative to the frame boundary, by **ten** periods (clock period number 2039) of **C16o**.
2. The channel control bit corresponding to Stream 12, Channel 0, **L/BSTo12_Ch0,** is transmitted on **L/BCSTo0** in advance of the frame boundary by **seven** periods (clock period number2042) of output clock, **C16o**. Similarly, the channel control bits for **L/BSTo13_Ch0**, **L/BSTo14_Ch0** and **L/BSTo15_Ch0** are advanced relative to the frame boundary by **seven** periods of **C16o**, on **L/BCSTo1**, **L/BCSTo2** and **L/BCSTo3**, respectively.
3. For stream **L/BSTo4,** the value of the channel control bit for **Channel 511** will be transmitted during the **$\overline{\text{C16o}}$** clock period number 2036 on **L/BCSTo0**.
4. For stream **L/BSTo5,** the value of the channel control bit for **Channel 5** will be transmitted during the **$\overline{\text{C16o}}$** clock period number 12 on **L/BCSTo1**.

	Allocated Stream No.				Channel No. [2]	
C16o Period[1]	L/BCSTo0	L/BCSTo1	L/BCSTo2	L/BCSTo3	32 Mbps	
2039	0 [3-1]	1	2	3	Ch 0	
2040	4	5	6	7	Ch 0	
2041	8	9	10	11	Ch 0	
2042	12 [3-2]	13 [3-2]	14 [3-2]	15 [3-2]	Ch 0	
2043	0	1	2	3	Ch 1	
2044	4	5	6	7	Ch 1	
2045	8	9	10	11	Ch 1	
2046	12	13	14	15	Ch 1	
2047	0	1	2	3	Ch 2	
2048	4	5	6	7	Ch 2	Frame
1	8	9	10	11	Ch 2	Boundary
2	12	13	14	15	Ch 2	
3	0	1	2	3	Ch 3	
4	4	5	6	7	Ch 3	
5	8	9	10	11	Ch 3	
6	12	13	14	15	Ch 3	
7	0	1	2	3	Ch 4	
8	4	5	6	7	Ch 4	
9	8	9	10	11	Ch 4	
10	12	13	14	15	Ch 4	
11	0	1	2	3	Ch 5	
12	4	5 [3-4]	6	7	Ch 5	
13	8	9	10	11	Ch 5	
14	12	13	14	15	Ch 5	
15	0	1	2	3	Ch 6	
16	4	5	6	7	Ch 6	
17	8	9	10	11	Ch 6	
etc.	etc.	etc.	etc.	etc.	etc.	
etc.	etc.	etc.	etc.	etc.	etc.	
2029	etc.	etc.	etc.	etc.	Ch 509	
2030	12	13	14	15	Ch 509	
2031	0	1	2	3	Ch 510	
2032	4	5	6	7	Ch 510	
2033	8	9	10	11	Ch 510	
2034	12	13	14	15	Ch 510	

Table 4 - L/BCSTo Allocation of Channel Control Bits to Output Streams (32 Mbps Mode)

	Allocated Stream No.				Channel No. [2]	
C16o Period[1]	L/BCSTo0	L/BCSTo1	L/BCSTo2	L/BCSTo3	32 Mbps	
2035	0	1	2	3	Ch 511	
2036	4[3-3]	5	6	7	Ch 511	
2037	8	9	10	11	Ch 511	
2038	12	13	14	15	Ch 511	
2039	0	1	2	3	Ch 0	
2040	4	5	6	7	Ch 0	
2041	8	9	10	11	Ch 0	
2042	12	13	14	15	Ch 0	
2043	0	1	2	3	Ch 1	
2044	4	5	6	7	Ch 1	
2045	8	9	10	11	Ch 1	
2046	12	13	14	15	Ch 1	
2047	0	1	2	3	Ch 2	
2048	4	5	6	7	Ch 2	Frame
1	8	9	10	11	Ch 2	Boundary
2	12	13	14	15	Ch 2	
3	0	1	2	3	Ch 3	
etc.	etc.	etc.	etc.	etc.	etc.	

Table 4 - L/BCSTo Allocation of Channel Control Bits to Output Streams (32 Mbps Mode) (continued)

Note 1: Clock period count is referenced to frame boundary.

Note 2: The channel numbers presented relate to the specific stream operating at a data rate of 32.768 Mbps.

Note 3: 3-1 to 3-4: See above for examples of channel control bits.

Figure 14, Local and Backplane Port External High Impedance Control Timing (32Mbps Mode) shows the channel control bits for **L/BCSTo0**, **L/BCSTo1**, **L/BCSTo2** and **L/BCSTo3**.

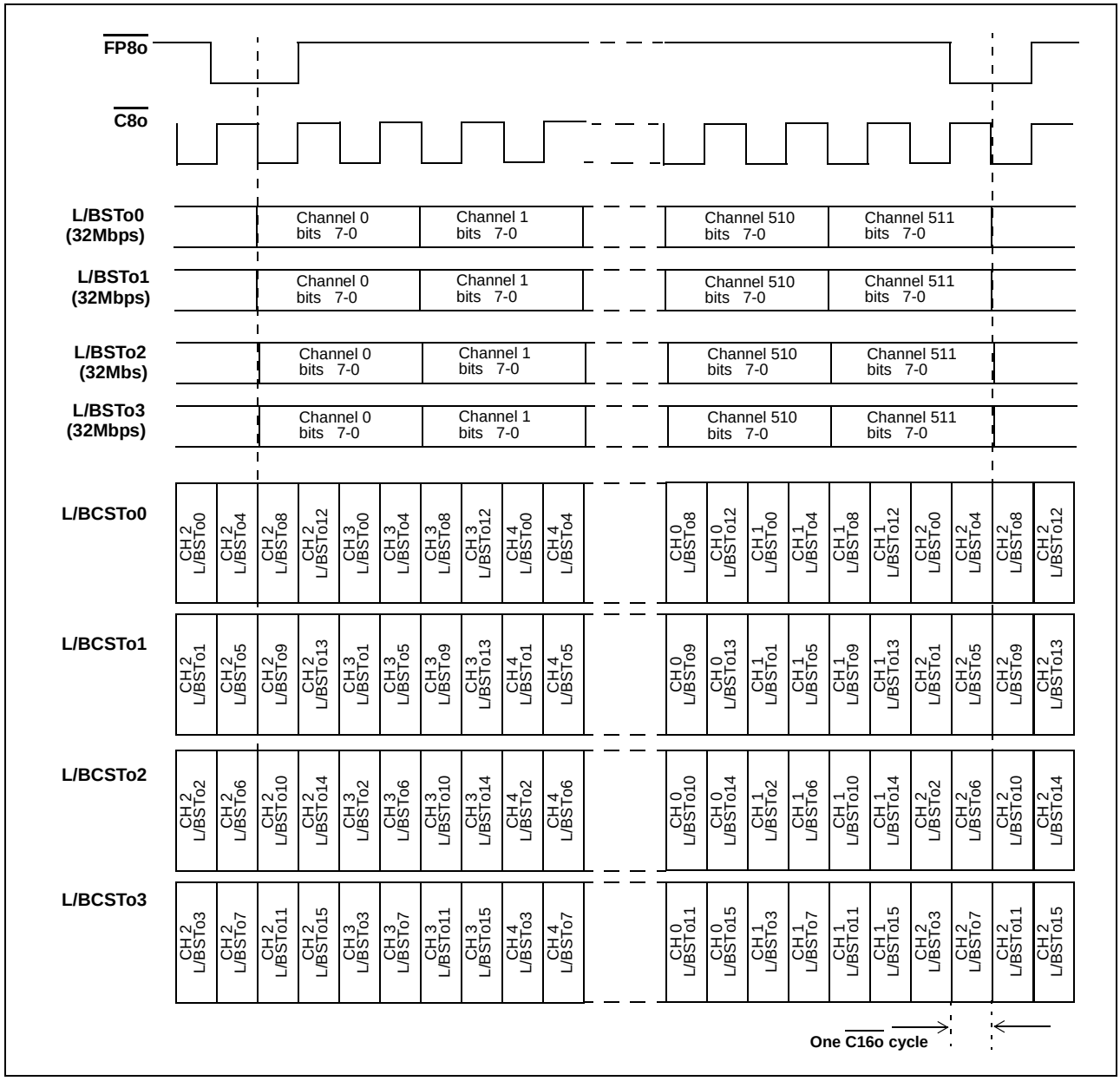


Figure 14 - Local and Backplane Port External High Impedance Control Timing (32Mbps Mode)

4.3 LORS/BORS Asserted HIGH

When the LORS/BORS input pin is HIGH, the Local/Backplane Output Enable Bit (**LE/BE**) of the Local/Backplane Connection Memory has direct per-channel control on the high impedance state of the Local/Backplane output streams, **L/BSTo0-31**. Programming a LOW state in the connection memory LE/BE bit will set the stream output of the device to high impedance for the duration of the channel period. See “Local Connection Memory Bit Definition,” on page 52 and “Backplane Connection Memory Bit Definition,” on page 53 for programming details.

When the LORS/BORS signal is asserted HIGH, the **L/BCSTo0-3** outputs directly the values given in LE/BE.

5.0 Data Delay Through the Switching Paths

Serial data which goes into the device is converted into parallel format and written to consecutive locations in the data memory. Each data memory location corresponds to the input stream and channel number. With the input channel delay feature disabled, channels written to any of the buffers during Frame N will be read out during Frame N+2. With the input channel delay feature enabled, channels written to any of the buffers during Frame N will be read out during Frame N+3.

The input channel offsets affect the overall throughput delay; however the input bit delay and output bit advancement have no impact on the overall data throughput delay.

In the following paragraphs, the data throughput delay (**T**) is represented as a function of ST-BUS frames, input channel number, (**m**), output channel number (**n**), and input channel delay (α). Table 5 describes the variable range for input streams and Table 6 describes the variable range for output streams. Table 7 summarizes the data throughput delay under various input channel and output channel delay conditions.

Input Stream Data Rate	Input Channel Number (m)	Possible Input channel delay (α)
2 Mbps	0 to 31	0 to 31
4 Mbps	0 to 63	0 to 63
8 Mbps	0 to 127	0 to 127
16 Mbps	0 to 255	0 to 255
32 Mbps	0 to 511	0 to 511

Table 5 - Variable Range for Input Streams

Output Stream Data Rate	Output Channel Number (n)
2 Mbps	0 to 31
4 Mbps	0 to 63
8 Mbps	0 to 127
16 Mbps	0 to 255
32 Mbps	0 to 511

Table 6 - Variable Range for Output Streams

Input Channel Delay OFF	Input Channel Delay ON
T = 2 frames + (n - m)	T = 3 frames - α + (n - m)

Table 7 - Data Throughput Delay

By default, when the input channel delay, α, is set to zero, the data throughput delay (**T**) is: **T = 2 frames + (n - m)**. Assuming that **m** (input channel) and **n** (output channel) are equal, we have the figure below, in which the delay between the input data being written and the output data being read is exactly 2 frames.

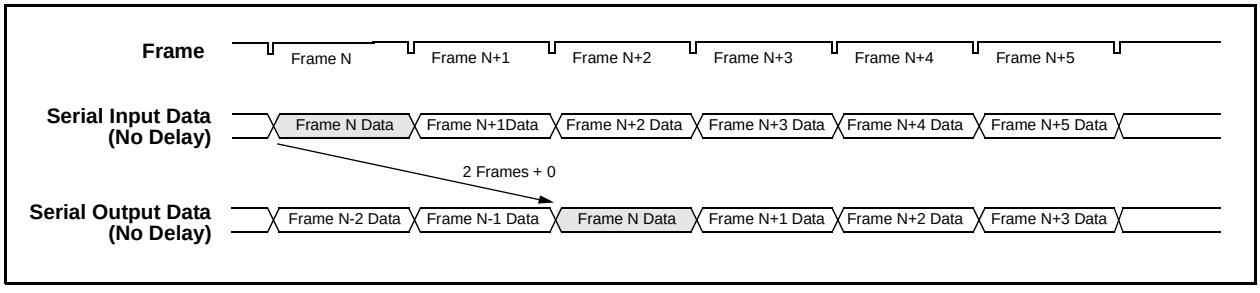


Figure 15 - Data Throughput Delay with Input Channel Delay Disabled, Input Ch0 Switched to Output Ch0

Assuming that **n** (output channel) is greater than **m** (input channel), we have the figure below, in which the delay time between the input channel being written and the output channel being read exceeds 2 frames.

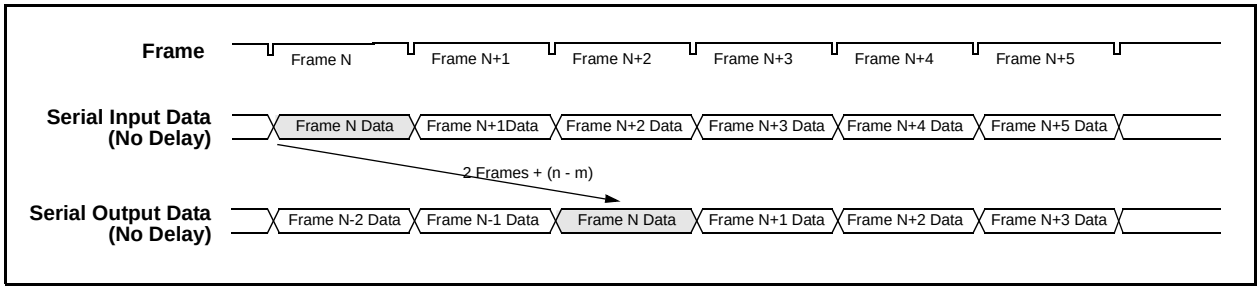


Figure 16 - Data Throughput Delay with Input Channel Delay Disabled, Input Ch0 Switched to Output Ch13

Assuming that **n** (output channel) is less than **m** (input channel), we have the figure below, in which the delay time between the input channel being written and the output channel being read is less than 2 frames.

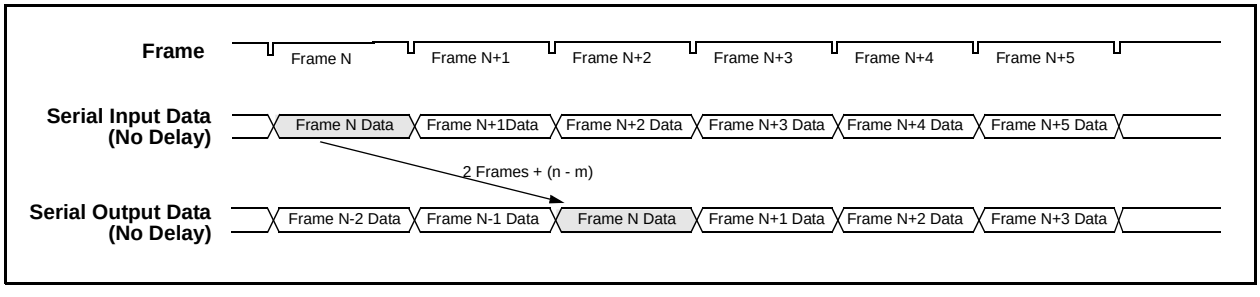


Figure 17 - Data Throughput Delay with Input Channel Delay Disabled, Input Ch13 Switched to Output Ch0

When the input channel delay, α, is enabled, the data throughput delay is: **T = 3 frames - α + (m - n)**. Assuming that **m** (input channel) and **n** (output channel) are equal, we have the figure below, in which the delay between the input data being written and the output data being read is less than 3 frames.

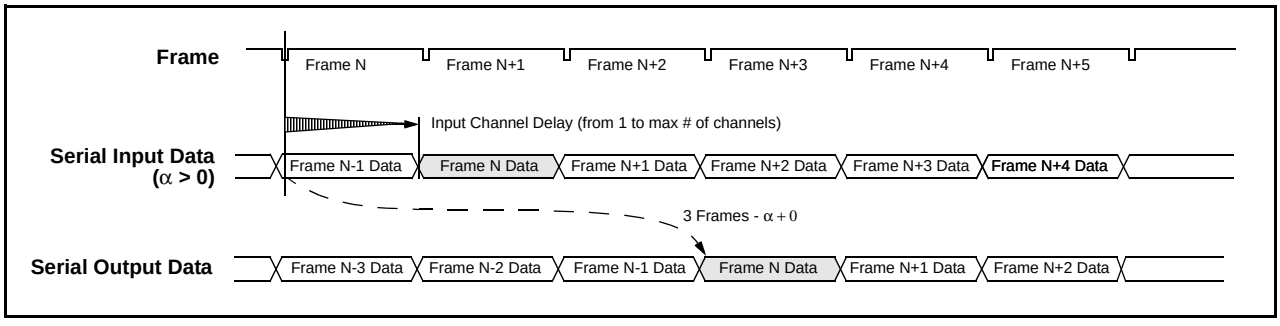


Figure 18 - Data Throughput Delay with Input Channel Delay Enabled, Input Ch0 Switched to Output Ch0

Assuming that **n** (output channel) is greater than **m** (input channel), we have the figure below, in which the delay time between the input channel being written and the output channel being read could exceed 3 frames, if the distance between n and m is greater than the input channel delay.

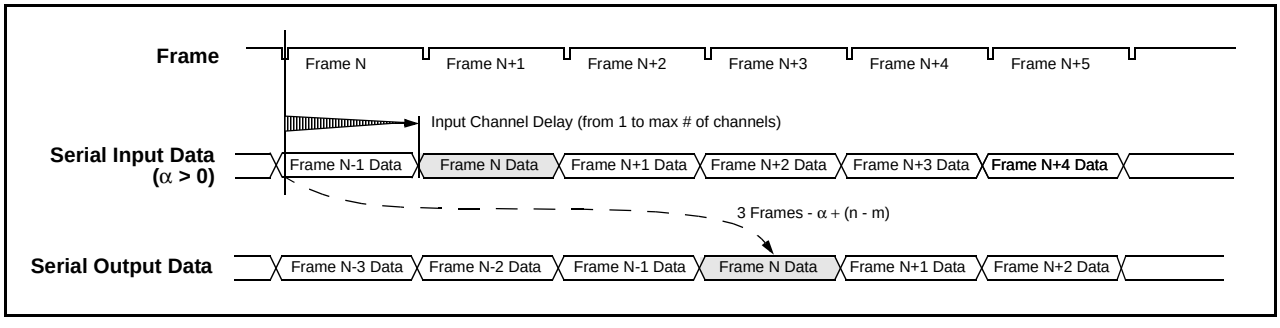


Figure 19 - Data Throughput Delay with Input Channel Delay Enabled, Input Ch0 Switched to Output Ch13

Assuming that **n** (output channel) is less than **m** (input channel), we have the figure below, in which the delay time between the input channel being written and the output channel being read will be less than 3 frames.

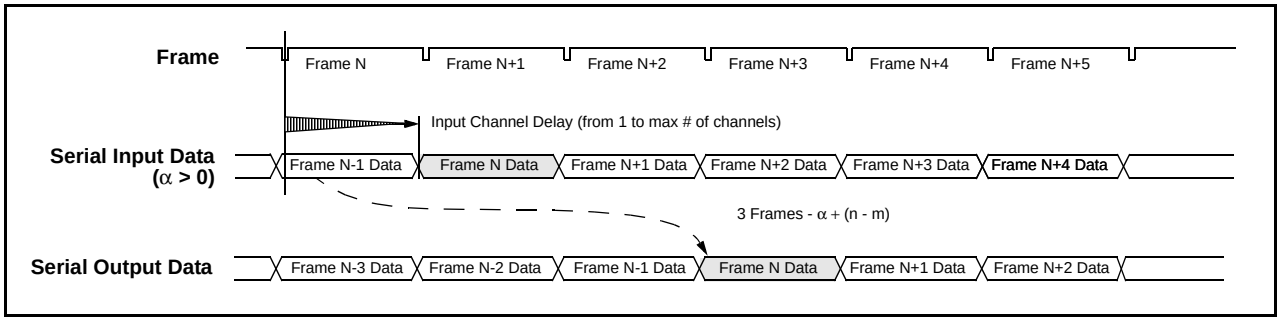


Figure 20 - Data Throughput Delay with Input Channel Delay Enabled, Input Ch13 Switched to Output Ch0

6.0 Bit Error Rate Test

Independent Bit Error Rate (BER) testers are provided for the Local and Backplane ports. In both ports there is a BER transmitter and a BER receiver. The transmitter and receiver are each independently controlled to allow Backplane-to-Backplane, Local-to-Local, Backplane-to-Local or Local-to-Backplane testing. The transmitter generates a 2^{15}-1 or 2^{23}-1 Pseudo Random Binary Sequence (PRBS), which may be allocated to a specific stream and number of channels. This is defined by a stream number, a start channel number, and the number of consecutive channels following the start channel. The stream, channel number and the number of consecutive channels following the start channel are similarly allocated for the receiver and detection of the PRBS. Examples of a channel sequence are presented in Figure 21.

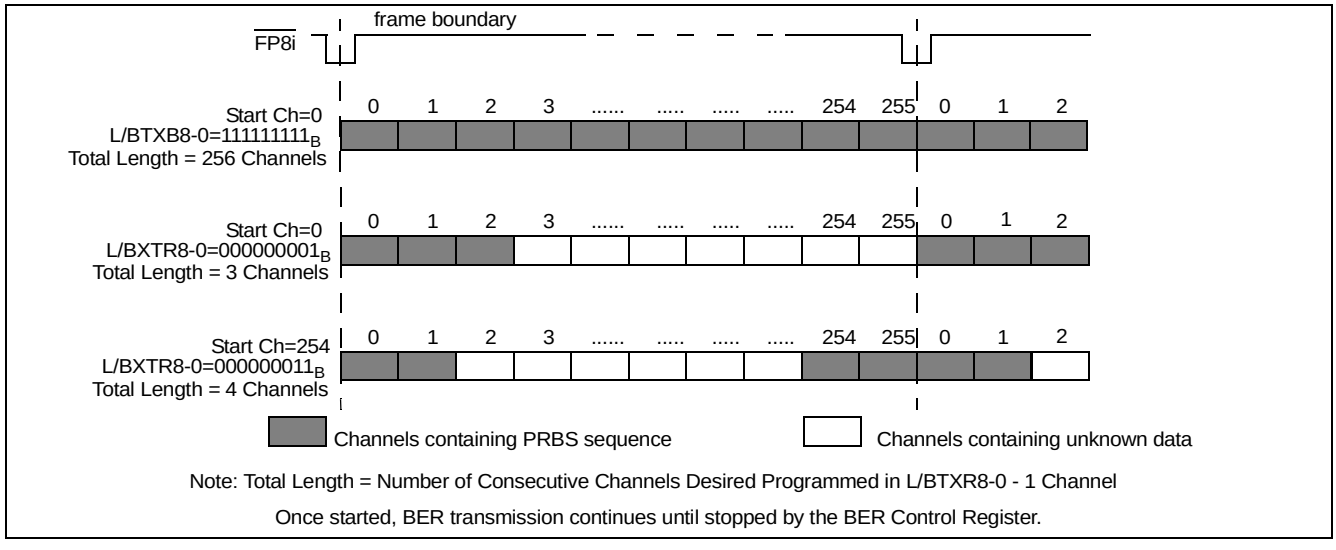


Figure 21 - Examples of BER Transmission Channels on a 16Mbps Output Stream

When enabled, the receiver attempts to lock to the PRBS on the incoming bit stream. Once lock is achieved, by detection of a seed value, a bit-by-bit comparison takes place and each error will increment a 16-bit counter. A counter saturation to $FFFF_H$ occurs in the event of an error count in excess of 65,535.

The BER operations are controlled by registers as follows (refer to Section 14.3, Bit Error Rate Test Control Register (BERCR) for overall control, Section 14.10, Local Bit Error Rate (BER) Registers and Section 14.11, Backplane Bit Error Rate (BER) Registers for register programming details):

- BER Control Register (**BERCR**) - Independently enables BER transmission and receive testing for Backplane and Local ports.
- Local and Backplane BER Start Send Registers (**LBSSR** and **BBSSR**) - Define the output stream and start channel for BER transmission.
- Local and Backplane Transmit BER Length Registers (**LTXBLR** and **BTXBLR**) - Define, for transmit stream, how many consecutive channels to follow the start channel.
- Local and Backplane BER Start Receive Registers (**LBSR** and **BBSR**) - Define the input stream and channel from which the BER sequence will start to be compared.
- Local and Backplane Receive BER Length Registers (**LRXBLR** and **BRXBLR**) - Define, for the receive stream, how many consecutive channels to follow the start channel.
- Local and Backplane BER Count Registers (**LBCR** and **BBCR**) - Contain the number of counted errors.

The registers listed completely define the transmit and receive stream and channels. When BER transmission is enabled for these channels, the source bits and the Message Mode bits, **LSRC** and **LMM** in the Local Connection Memory, and **BSRC** and **BMM** in the Backplane Connection Memory, are ignored. The per-channel enable bits (**LE**

and **BE**) of the respective connection memories should be set to HIGH to enable the outputs for the selected channels.

The BER receive channel numbering is not affected by the input channel delay value. It means that the BER receive circuitry always assume there is no input channel delay, regardless of the values of the **BCDR** and **LCDR** registers. For example, if BER data is received on local input stream 0 channel 3, without input channel delay, the LBSRR (Local BER Start Receive Register) should be programmed to 3. With input channel delay of 5, however, the LBSRR should be programmed to 8 (3 + 5) instead.

Note that when BER transmission is enabled, the target channels will carry PRBS data, and the rest of the channels on all streams of the same side (Local/Backplane) will carry unknown data, which renders that side of the switch unable to switch traffic during BER test.

7.0 Microprocessor Port

The 16 K switch family supports non-multiplexed Motorola type microprocessor buses. The microprocessor port consists of a 16-bit parallel data bus (**D0-15**), a 15-bit address bus (**A0-14**) and four control signals (**CS, DS, R/W** and **DTA**). The data bus provides access to the internal registers, the Backplane Connection and Data Memories, and the Local Connection and Data Memories. Each memory has 8,192 locations. See Table 11, Address Map for Data and Connection Memory Locations (A14 = 1), for the address mapping.

Each Connection Memory can be read or written via the 16-bit microprocessor port. The Data Memories can only be read (but not written) from the microprocessor port.

To prevent the bus 'hanging', in the event of the switch not receiving a master clock, the microprocessor port shall complete the $\overline{\text{DTA}}$ handshake when accessed, but any data read from the bus will be invalid.

8.0 Device Power-up, Initialization and Reset

8.1 Power-Up Sequence

The recommended power-up sequence is for the V_{DD_IO} supply (nominally +3.3 V) to be established before the power-up of the V_{DD_PLL} and V_{DD_CORE} supplies (nominally +1.8 V). The V_{DD_PLL} and V_{DD_CORE} supplies may be powered up simultaneously, but neither should 'lead' the V_{DD_IO} supply by more than 0.3 V.

All supplies may be powered-down simultaneously.

8.2 Initialization

Upon power up, the device should be initialized by applying the following sequence:

1 Ensure the $\overline{\textbf{TRST}}$ pin is permanently LOW to disable the JTAG TAP controller.

2 Set **ODE** pin to LOW. This configures the **LCSTo0-3** output signals to LOW (i.e., setting optional external output buffers to high impedance), and sets the **LSTo0-31** outputs to HIGH or high impedance, dependent on the **LORS** input value, and sets the **BCSTo0-3** output signals to LOW (i.e., setting optional external output buffers to high impedance), and sets the **BSTo0-31** outputs to HIGH or high impedance, dependent on **BORS** input value. Refer to Pin Description for details of the **LORS** and **BORS** pins.

3 Reset the device by asserting the $\overline{\textbf{RESET}}$ pin to zero for at least two cycles of the input clock, $\overline{\textbf{C8i}}$. A delay of an additional 250 µs must also be applied before the first microprocessor access is performed following the de-assertion of the **RESET** pin; this delay is required for determination of the input frame pulse format.

4 Use the Block Programming Mode to initialize the Local and the Backplane Connection Memories. Refer to Section 9.3, Connection Memory Block Programming.

5 Set **ODE** pin to HIGH after the connection memories are programmed to ensure that bus contention will not occur at the serial stream outputs.

8.3 Reset

The **RESET** pin is used to reset the device. When set LOW, an asynchronous reset is applied to the device. It is then synchronized to the internal clock. During the reset period, depending on the state of input pins **LORS** and **BORS**, the output streams **LSTo0-31** and **BSTo0-31** are set to HIGH or high impedance, and all internal registers and counters are reset to the default state.

The **RESET** pin must remain LOW for two input clock cycles (**C8i**) to guarantee a synchronized reset release. A delay of an additional 250 µs must also be waited before the first microprocessor access is performed following the de-assertion of the **RESET** pin; this delay is required for determination of the frame pulse format.

In addition, the reset signal must be de-asserted less than 12µs after the frame boundary or more than 13 µs after the frame boundary, as illustrated in Figure 22. This can be achieved, for example, by synchronizing the de-assertion of the reset signal with the input frame pulse **FP8i**.

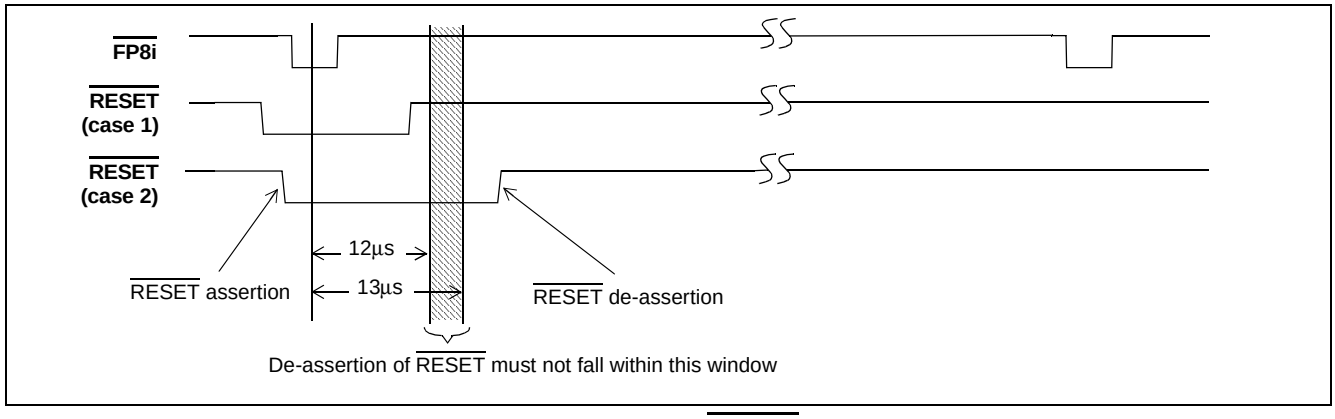


Figure 22 - Hardware RESET de-assertion

9.0 Connection Memory

The device includes two connection memories, the Local Connection Memory and the Backplane Connection Memory.

9.1 Local Connection Memory

The Local Connection Memory (LCM) is a 16-bit wide memory with 8,192 memory locations to support the Local output port. The most significant bit of each word, bit[15], selects the source stream from either the Backplane (LSRC = LOW) or the Local (LSRC = HIGH) port and determines the Backplane-to-Local or Local-to-Local data routing. Bits[14:13] select the control modes of the Local output streams, the per-channel Message Mode and the per-channel high impedance output control modes. In Connection Mode (bit[14] = LOW), bits[12:0] select the source stream and channel number as detailed in Table 8. In Message Mode (bit[14] = HIGH), bits[12:8] are unused and bits[7:0] contain the message byte to be transmitted. Bit[13] must be HIGH for Message Mode to ensure that the output channel is not tri-stated.

9.2 Backplane Connection Memory

The Backplane Connection Memory (BCM) is a 16-bit wide memory with 8,192 memory locations to support the Backplane output port. The most significant bit of each word, bit[15], selects the source stream from either the Backplane (BSRC = HIGH) or the Local (BSRC = LOW) port and determines the Local-to-Backplane or Backplane-to-Backplane data routing. Bit[14:13] select the control modes of the Backplane output streams, namely the per-channel Message Mode and the per-channel high impedance output control mode. In Connection Mode (bit[14] = LOW), bits[12:0] select the source stream and channel number as detailed in Table 8. In Message Mode (bit[14] = HIGH), bits[12:8] are unused and bits[7:0] contain the message byte to be transmitted. Bit[13] must be HIGH for Message Mode to ensure that the output channel is not tri-stated.

The Control Register bits MS[2:0] must be set to 000 to select the Local Connection Memory for the write and read operations via the microprocessor port. The Control Register bits MS[2:0] must be set to 001 to select the Backplane Connection Memory for the write and read operations via the microprocessor port. See Section 7.0, Microprocessor Port, and Section 14.1, Control Register (CR) for details on microprocessor port access.

Source Stream Bit Rate	Source Stream No.	Source Channel No.
2 Mbps	Bits[12:8] legal values 0:31	Bits[7:0] legal values 0:31
4 Mbps	Bits[12:8] legal values 0:31	Bits[7:0] legal values 0:63
8 Mbps	Bits[12:8] legal values 0:31	Bits[7:0] legal values 0:127
16 Mbps	Bits[12:8] legal values 0:31	Bits[7:0] legal values 0:255
32 Mbps	Bits[12:9] legal values 0:15	Bits[8:0] legal values 0:511

Table 8 - Local and Backplane Connection Memory Configuration

9.3 Connection Memory Block Programming

This feature allows fast, simultaneous, initialization of the Local and Backplane Connection Memories after power-up. When the Memory Block Programming mode is enabled, the contents of the Block Programming Register (BPR) will be loaded into the connection memories. See Table 19 and Table 20 for details of the Control Register and Block Programming Register values, respectively.

9.3.1 Memory Block Programming Procedure:

- Set the **MBP** bit in the Control Register from LOW to HIGH.
- Set the **BPE** bit to HIGH in the Block Programming Register (BPR). The Local Block Programming data bits, **LBPD[2:0]**, of the Block Programming Register, will be loaded into bits[15:13] of the Local Connection Memory. The remaining bit positions are loaded with zeros as shown in Table 9.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LBPD2	LBPD1	LBPD0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 9 - Local Connection Memory in Block Programming Mode

The Backplane Block Programming data bits, **BBPD[2:0]**, of the Block Programming Register, will be loaded into bits[15:13] respectively, of the Backplane Connection Memory. The remaining bit positions are loaded with zeros as shown in Table 10.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BBPD2	BBPD1	BBPD0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 10 - Backplane Connection Memory in Block Programming Mode

The Block Programming Register bit, **BPE** will be automatically reset LOW within 125 µs, to indicate completion of memory programming.

The Block Programming Mode can be terminated at any time prior to completion by clearing the **BPE** bit of the Block Programming Register or the **MBP** bit of the Control Register.

Note that the default values (LOW) of **LBPD[2:0]** and **BBPD[2:0]** of the Block Programming Register, following a device reset, can be used.

During reset, all output channels go HIGH or high impedance, depending on the value of the LORS and BORS pins, irrespective of the values in bits[14:13] of the connection memory.

10.0 Memory Built-In-Self-Test (BIST) Mode

As operation of the memory BIST will corrupt existing data, this test must only be initiated when the device is placed “out-of-service” or isolated from live traffic.

The memory BIST mode is enabled through the microprocessor port (Section 14.14, Memory BIST Register). Internal BIST memory controllers generate the memory test pattern (S-march) and control the memory test. The memory test result is monitored through the Memory BIST Register.

11.0 JTAG Port

The ZL50060/1 JTAG interface conforms to the IEEE 1149.1 standard. The operation of the boundary-scan circuit shall be controlled by an external Test Access Port (TAP) Controller.

11.1 Test Access Port (TAP)

The Test Access Port (TAP) consists of four input pins and one output pin described as follows:

- **Test Clock Input (TCK)**
  TCK provides the clock for the TAP Controller and is independent of any on-chip clock. **TCK** permits the shifting of test data into or out of the Boundary-Scan register cells under the control of the TAP Controller in Boundary-Scan Mode.
- **Test Mode Select Input (TMS)**
  The TAP controller uses the logic signals applied to the **TMS** input to control test operations. The TMS signals are sampled at the rising edge of the **TCK** pulse. This pin in internally pulled to V_{DD_IO} when not driven from an external source.
- **Test Data Input (TDi)**
  Depending on the previously applied data to the **TMS** input, the serial input data applied to the **TDi** port is connected either to the Instruction Register or to a Test Data Register. Both registers are described in Section 11.2, TAP Registers. The applied input data is sampled at the rising edge of **TCK** pulses. This pin is internally pulled to V_{DD_IO} when not driven from an external source.
- **Test Data Output (TDo)**
  Depending on the previously applied sequence to the **TMS** input, the contents of either the instruction register or data register are serially shifted out towards the **TDo**. The data out of the **TDo** is clocked on the

falling edge of the **TCK** pulses. When no data is shifted through the boundary scan cells, the **TDo** output is set to a high impedance state.

- **Test Reset ($\overline{\text{TRST}}$)**
  TRST provides an asynchronous Reset to the JTAG scan structure. This pin is internally pulled high when not driven from an external source. This pin MUST be pulled low for normal operation.

11.2 TAP Registers

The ZL50060/1 implements the public instructions defined in the IEEE-1149.1 standard with the provision of an Instruction Register and three Test Data Registers.

11.2.1 Test Instruction Register

The JTAG interface contains a four-bit instruction register. Instructions are serially loaded into the Instruction Register from the **TDi** pin when the TAP Controller is in the shift-IR state. Instructions are subsequently decoded to achieve two basic functions: to select the Test Data Register to operate while the instruction is current, and to define the serial Test Data Register path to shift data between **TDi** and **TDo** during data register scanning. Please refer to Figure 34 for JTAG test port timing.

11.2.2 Test Data Registers

11.2.2.1 The Boundary-Scan Register

The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the ZL50060/1 core logic.

11.2.2.2 The Bypass Register

The Bypass register is a single stage shift register to provide a one-bit path from **TDi** to **TDo**.

11.2.2.3 The Device Identification Register

The JTAG device ID for the ZL50060/1 is $0C38D14B_H$.

Version, Bits <31:28>:0000

Part No., Bits <27:12>:1100 0011 1000 1101

Manufacturer ID, Bits <11:1>:0001 0100 101

Header, Bit <0> (LSB):1

11.3 Boundary Scan Description Language (BSDL) File

A Boundary Scan Description Language (BSDL) file is available from Zarlink Semiconductor to aid in the use of the IEEE 1149.1 test interface.

12.0 Memory Address Mappings

When the most significant bit, A14, of the address bus is set to '1', the microprocessor performs an access to one of the device's internal memories. The Control Register bits MS[2:0] indicate which memory (Local Connection, Local Data, Backplane Connection, or Backplane Data) is being accessed. Address bits A0-A13 indicate which location within the particular memory is being accessed.

Address Bit	Description
A14	Selects memory or register access (0 = register, 1 = memory). Note that which memory (Local Connection, Local Data, Backplane Connection, Backplane Data) is accessed depends on the **MS[2:0] bits in the Control Register**.
A13-A9	Stream address (0 - 31) Only streams 0 to 15 are used when the target side (Local/Backplane) is operating at 32.768Mbps.
A8-A0	Channel address (0 - 511) Channels 0 to 31 are used when serial stream is at 2.048 Mbps Channels 0 to 63 are used when serial stream is at 4.096 Mbps Channels 0 to 127 are used when serial stream is at 8.192 Mbps Channels 0 to 255 are used when serial stream is at 16.384 Mbps Channels 0 to 511 are used when serial stream is at 32.768 Mbps

Table 11 - Address Map for Data and Connection Memory Locations (A14 = 1)

The device contains two data memory blocks, one for received Backplane data and one for received Local data. For all data rates, the received data is converted to parallel format by internal serial-to-parallel converters and stored sequentially in the relevant data memory.

12.1 Local Data Memory Bit Definition

The 8-bit Local Data Memory (LDM) has 8,192 positions. The locations are associated with the Local input streams and channels. As explained in the section above, address bits A13-A0 of the microprocessor define the addresses of the streams and the channels. The LDM is read-only and configured as follows:

Bit	Name	Description
15:8	Reserved	Set to a default value of 8'h00.
7:0	LDM	**Local Data Memory - Local Input Channel Data.** The LDM[7:0] bits contain the timeslot data from the Local side input TDM stream. LDM[7] corresponds to the first bit received, i.e., bit 7 in ST-BUS mode, bit 0 in GCI-Bus mode. See Figure 7, ST-BUS and GCI-Bus Input Timing Diagram for Different Data Rates for the arrival order of the bits.

Table 12 - Local Data Memory (LDM) Bits

Note that the Local Data Memory is actually an 8-bit wide memory. The most significant 8 bits expressed in the table above are presented to provide 16-bit microprocessor read accesses.

12.2 Backplane Data Memory Bit Definition

The 8-bit Backplane Data Memory (BDM) has 8,192 positions. The locations are associated with the Backplane input streams and channels. As explained previously, address bits A13-A0 of the microprocessor define the addresses of the streams and the channels. The BDM is read-only and configured as follows:

Bit	Name	Description
15:8	Reserved	Set to a default value of 8'h00.
7:0	BDM	**Backplane Data Memory - Backplane Input Channel Data.** The BDM[7:0] bits contain the timeslot data from the Backplane side input TDM stream. BDM[7] corresponds to the first bit received, i.e., bit 7 in ST-BUS mode, bit 0 in GCI-Bus mode. See Figure 7, ST-BUS and GCI-Bus Input Timing Diagram for Different Data Rates for the arrival order of the bits

Table 13 - Backplane Data Memory (BDM) Bits

Note that the Backplane Data Memory is actually an 8-bit wide memory. The most significant 8 bits expressed in the table above are presented to provide 16-bit microprocessor read accesses.

12.3 Local Connection Memory Bit Definition

The Local Connection Memory (LCM) has 8,192 addresses of 16-bit words. Each address, accessed through bits A13-A0 of the microprocessor port, is allocated to an individual Local output stream and channel. The bit definition for each 16-bit word is presented in Table 14 for Non-32 Mbps Source-to-Local Mode connections, and in Table 15 for 32Mbps Source-to-Local Mode connections.

The most-significant bit in the memory location, LSRC, selects the switch configuration for Backplane-to-Local or Local-to-Local. When the per-channel Message Mode is selected (LMM memory bit = HIGH), the lower byte of the LCM word (LCAB[7:0]) will be transmitted as data on the output stream (LSTo0-31) in place of data defined by the Source Control, Stream and Channel Address bits.

Bit	Name	Description
15	LSRC	**Local Source Control Bit** When LOW, the source is from the Backplane input port (Backplane Data Memory). When HIGH, the source is from the Local input port (Local Data Memory). Ignored when LMM is set HIGH.
14	LMM	**Local Message Mode Bit** When LOW, the channel is in Connection Mode (data to be output on channel originated in Local or Backplane Data Memory). When HIGH, the channel is in Message Mode (data to be output on channel originated in Local Connection Memory).
13	LE	**Local Output Enable Bit** When LOW, the channel may be high impedance, either at the device output, or set by an external buffer dependent upon the LORS pin. When HIGH, the channel is active.
12:8	LSAB[4:0]	**Source Stream Address Bits** The binary value of these 5 bits represents the input stream number. Ignored when LMM is set HIGH.

Table 14 - LCM Bits for Non-32Mbps Source-to-Local Switching

Bit	Name	Description
7:0	LCAB[7:0]	**Source Channel Address Bits / Message Mode Data** The binary value of these 8 bits represents the input channel number when LMM is set LOW. Transmitted as data when LMM is set HIGH. Note: When LMM is set HIGH, in both ST-BUS and GCI-Bus modes, the LCAB[7:0] bits are output sequentially to the timeslot with LCAB[7] being output first.

Table 14 - LCM Bits for Non-32Mbps Source-to-Local Switching (continued)

Bit	Name	Description
15	LSRC	**Local Source Control Bit** When LOW, the source is from the Backplane input port (Backplane Data Memory). When HIGH, the source is from the Local input port (Local Data Memory). Ignored when LMM is set HIGH.
14	LMM	**Local Message Mode Bit** When LOW, the channel is in Connection Mode (data to be output on channel originated in Local or Backplane Data Memory). When HIGH, the channel is in Message Mode (data to be output on channel originated in Local Connection Memory).
13	LE	**Local Output Enable Bit** When LOW, the channel may be high impedance, either at the device output, or set by an external buffer dependent upon the LORS pin. When HIGH, the channel is active.
12:9	LSAB[3:0]	**Source Stream Address Bits** The binary value of these 4 bits represents the input stream number. Ignored when LMM is set HIGH.
8:0	LCAB[8:0]	**Source Channel Address Bits / Message Mode Data** The binary value of these 9 bits represents the input channel number, when LMM is LOW. Bits LCAB[7:0] transmitted as data when LMM is set HIGH. Note: When LMM is set HIGH, in both ST-BUS and GCI-Bus modes, the LCAB[7:0] bits are output sequentially to the timeslot with LCAB[7] being output first.

Table 15 - LCM Bits for 32Mbps Source-to-Local Switching

12.4 Backplane Connection Memory Bit Definition

The Backplane Connection Memory (BCM) has 8,192 addresses of 16-bit words. Each address, accessed through bits A13-A0 of the microprocessor port, is allocated to an individual Backplane output stream and channel. The bit definition for each 16-bit word is presented in Table 16 for Non-32 Mbps Source-to-Backplane Mode connections, and in Table 17 for 32 Mbps Source-to-Backplane Mode connections.

The most-significant bit in the memory location, BSRC, selects the switch configuration for Local-to-Backplane or Backplane-to-Backplane. When the per-channel Message Mode is selected (BMM memory bit = HIGH), the lower byte of the BCM word (BCAB[7:0]) will be transmitted as data on the output stream (BSTo0-31) in place of data defined by the Source Control, Stream and Channel Address bits.

Bit	Name	Description
15	BSRC	**Backplane Source Control Bit** When LOW, the source is from the Local input port (Local Data Memory). When HIGH, the source is from the Backplane input port (Backplane Data Memory). Ignored when BMM is set HIGH.
14	BMM	**Backplane Message Mode Bit** When LOW, the channel is in Connection Mode (data to be output on channel originated in Backplane or Local Data Memory). When HIGH, the channel is in Message Mode (data to be output on channel originated in Backplane Connection Memory).
13	BE	**Backplane Output Enable Bit** When LOW, the channel may be high impedance, either at the device output, or set by an external buffer dependent upon the BORS pin. When HIGH, the channel is active.
12:8	BSAB[4:0]	**Source Stream Address Bits** The binary value of these 5 bits represents the input stream number. Ignored when BMM is set HIGH.
7:0	BCAB[7:0]	**Source Channel Address Bits / Message Mode Data** The binary value of these 8 bits represents the input channel number when BMM is set LOW. Transmitted as data when BMM is set HIGH. Note: When BMM is set HIGH, in both ST-BUS and GCI-Bus modes, the BCAB[7:0] bits are output sequentially to the timeslot with BCAB[7] being output first.

Table 16 - BCM Bits for Non-32Mbps Source-to-Backplane Switching

Bit	Name	Description
15	BSRC	**Backplane Source Control Bit** When LOW, the source is from the Local input port (Local Data Memory). When HIGH, the source is from the Backplane input port (Backplane Data Memory). Ignored when BMM is set HIGH.
14	BMM	**Backplane Message Mode Bit** When LOW, the channel is in Connection Mode (data to be output on channel originated in Backplane or Local Data Memory). When HIGH, the channel is in Message Mode (data to be output on channel originated in Backplane Connection Memory).
13	BE	**Backplane Output Enable Bit** When LOW, the channel may be high impedance, either at the device output, or set by an external buffer dependent upon the BORS pin. When HIGH, the channel is active.
12:9	BSAB[3:0]	**Source Stream Address Bits** The binary value of these 4 bits represents the input stream number. Ignored when BMM is set HIGH.

Bit	Name	Description
8:0	BCAB[8:0]	**Source Channel Address Bits / Message Mode Data** The binary value of these 9 bits represents the input channel number, when BMM is LOW. Bits BCAB[7:0] transmitted as data when BMM is set HIGH. Note: When BMM is set HIGH, in both ST-BUS and GCI-Bus modes, the BCAB[7:0] bits are output sequentially to the timeslot with BCAB[7] being output first.

Table 17 - BCM Bits for 32Mbps Source-to-Backplane Switching

13.0 Internal Register Mappings

When the most significant bit, A14, of the address bus is set to '0', the microprocessor is performing an access to one of the device's internal registers. Address bits A13-A0 indicate which particular register is being accessed.

A14-A0	Register
0000_H	Control Register, CR
0001_H	Block Programming Register, BPR
0002_H	BER Control Register, BERCR
0003_H - 0022_H	Local Input Channel Delay Register 0 - 31, LCDR0 - 31
0023_H - 0042_H	Local Input Bit Delay Register 0 - 31, LIDR0 - 31
0043_H - 0062_H	Backplane Input Channel Delay Register 0 - 31, BCDR0 - 31
0063_H - 0082_H	Backplane Input Bit Delay Register 0 - 31, BIDR0 - 31
0083_H - $00A2_H$	Local Output Advancement Register 0 - 31, LOAR0 - 31
$00A3_H$ - $00C2_H$	Backplane Output Advancement Register 0 - 31, BOAR0 - 31
$00C3_H$	Local BER Start Send Register, LBSSR
$00C4_H$	Local Transmit BER Length Register, LTXBLR
$00C5_H$	Local Receive BER Length Register, LRXBLR
$00C6_H$	Local BER Start Receive Register, LBSRR
$00C7_H$	Local BER Count Register, LBCR
$00C8_H$	Backplane BER Start Send Register, BBSSR
$00C9_H$	Backplane Transmit BER Length Register, BTXBLR
$00CA_H$	Backplane Receive BER Length Register, BRXBLR
$00CB_H$	Backplane BER Start Receive Register, BBSRR
$00CC_H$	Backplane BER Count Register, BBCR
$00CD_H$ - $00EC_H$	Local Input Bit Rate Register 0 - 31, LIBRR0 - 31
$00ED_H$ - $010C_H$	Local Output Bit Rate Register 0 - 31, LOBRR0 - 31
$010D_H$ - $012C_H$	Backplane Input Bit Rate Register 0 - 31, BIBRR0 - 31

Table 18 - Address Map for Registers (A14 = 0)

A14-A0	Register
$012D_H$ - $014C_H$	Backplane Output Bit Rate Register 0 - 31, BOBRR0 - 31
$014D_H$	Memory BIST Register, MBISTR
$3FFF_H$	Device Identification Register, DIR

Table 18 - Address Map for Registers (A14 = 0) (continued)

14.0 Detailed Register Descriptions

This section describes the registers that are used in the device.

14.1 Control Register (CR)

Address 0000_H.

The Control Register defines which memory is to be accessed. It initiates the memory block programming mode and selects the Backplane and Local data rate modes. The Control Register (**CR**) is configured as follows:

Bit	Name	Reset Value	Description
15:13	FBD_ MODE[2:0]	0	**Frame Boundary Discriminator Mode** When set to 111_B, the Frame Boundary Discriminator can handle both low frequency and high frequency jitter. When set to 000_B, the Frame Boundary Discriminator is set to handle lower frequency jitter only. All other values are reserved. These bits are ignored when FBDEN bit is LOW.
12	SMPL_ MODE	0	**Sample Point Mode** When LOW the input bit sampling point is always at the 3/4 bit location. The input bit fractional delay is programmed in 1/4 bit increments from 0 to 7 3/4 as per the value of the LIDR0 to LIDR31 and BIDR0 to BIDR31 registers. When HIGH, the input bit sampling point is programmed to the 3/4, 4/4, 1/4, 2/4 bit location as per the value of the LIDR0 to LIDR31 and BIDR0 to BIDR31 registers. In addition, the incoming data can be delayed by 0 to 7 bits in 1 bit increments. See Table 24, Table 25, Table 28 and Table 29 for details.
11	Reserved	0	**Reserved** Must be set to 0 for normal operation
10	FBDEN	0	**Frame Boundary Discriminator Enable** When LOW, the frame boundary discriminator function is disabled. When HIGH, enables frame boundary discriminator function which allows the device to tolerate inconsistent frame boundaries, hence improving the tolerance to cycle-to-cycle variation on the input clock.
9	MODE32L	0	**Local 32MHz Mode** When LOW, Local streams LSTi0-31 and LSTo0-31 can be individually programmed for data rates of 2, 4, 8, or 16 Mbps. When HIGH, Local streams LSTi0-15 and LSTo0-15 operate at 32.768 Mbps only and LSTi16-31 and LSTo16-31 are unused.

Table 19 - Control Register Bits

<table>
<tr><th>Bit</th><th>Name</th><th>Reset Value</th><th>Description</th></tr>
<tr><td>8</td><td>FPW</td><td>0</td><td>Frame Pulse Width
When LOW, the user must apply a 122 ns frame pulse on FP8i; the FP8o pin will output a 122 ns wide frame pulse; FP16o will output a 61 ns wide frame pulse.
When HIGH, the user must apply a 244 ns frame pulse on FP8i; the FP8o pin will output a 244 ns wide frame pulse; FP16o will output a 122 ns wide frame pulse.</td></tr>
<tr><td>7</td><td>MODE32B</td><td>0</td><td>Backplane 32 MHz Mode
When LOW, Backplane streams BSTi0-31 and BSTo0-31 may be individually programmed for data rates of 2, 4, 8, or 16 Mbps.
When HIGH, Backplane streams BSTi0-15 and BSTo0-15 operate at 32.768 Mbps only and BSTi16-31 and BSTo16-31 are unused.</td></tr>
<tr><td>6</td><td>C8IPOL</td><td>0</td><td>8 MHz Input Clock Polarity
The frame boundary is aligned to the falling or rising edge of the input clock.
When LOW, the frame boundary is aligned to the clock falling edge.
When HIGH, the frame boundary is aligned to the clock rising edge.</td></tr>
<tr><td>5</td><td>COPOL</td><td>0</td><td>Output Clock Polarity
When LOW, the output clock has the same polarity as the input clock.
When HIGH, the output clock is inverted.
This applies to both the 8 MHz (C8o) and 16 MHz (C16o) output clocks.</td></tr>
<tr><td>4</td><td>MBP</td><td>0</td><td>Memory Block Programming
When LOW, the memory block programming mode is disabled.
When HIGH, the connection memory block programming mode is ready to program the Local Connection Memory (LCM) and the Backplane Connection Memory (BCM).</td></tr>
<tr><td>3</td><td>OSB</td><td>0</td><td>Output Stand By
This bit enables the BSTo0-31 and LSTo0-31 serial outputs.
<table><tr><th>ODE Pin</th><th>OSB bit</th><th>BSTo0-31, LSTo0-31</th></tr><tr><td>0</td><td>X</td><td>Disabled</td></tr><tr><td>1</td><td>0</td><td>Disabled</td></tr><tr><td>1</td><td>1</td><td>Enabled</td></tr></table>Output Control with ODE pin and OSB bit

When LOW, BSTo0-31 and LSTo0-31 are driven HIGH or high impedance, dependent on the BORS and LORS pin settings respectively, and BCSTo0-3 and LCSTo0-3 are driven low.
When HIGH, BSTo0-31, LSTo0-31, BCSTo0-3 and LCSTo0-3 are enabled.</td></tr>
<tr><td>2</td><td>Reserved</td><td>0</td><td>Reserved
Must be set to 0 for normal operation</td></tr>
<tr><td>1:0</td><td>MS[1:0]</td><td>0</td><td>Memory Select Bits
These three bits select the connection or data memory for subsequent microport memory access operations:
00 selects Local Connection Memory (LCM) for read or write operations.
01 selects Backplane Connection Memory (BCM) for read or write operations.
10 selects Local Data Memory (LDM) for read-only operation.
11 selects Backplane Data Memory (BDM) for read-only operation.</td></tr>
</table>

Table 19 - Control Register Bits (continued)

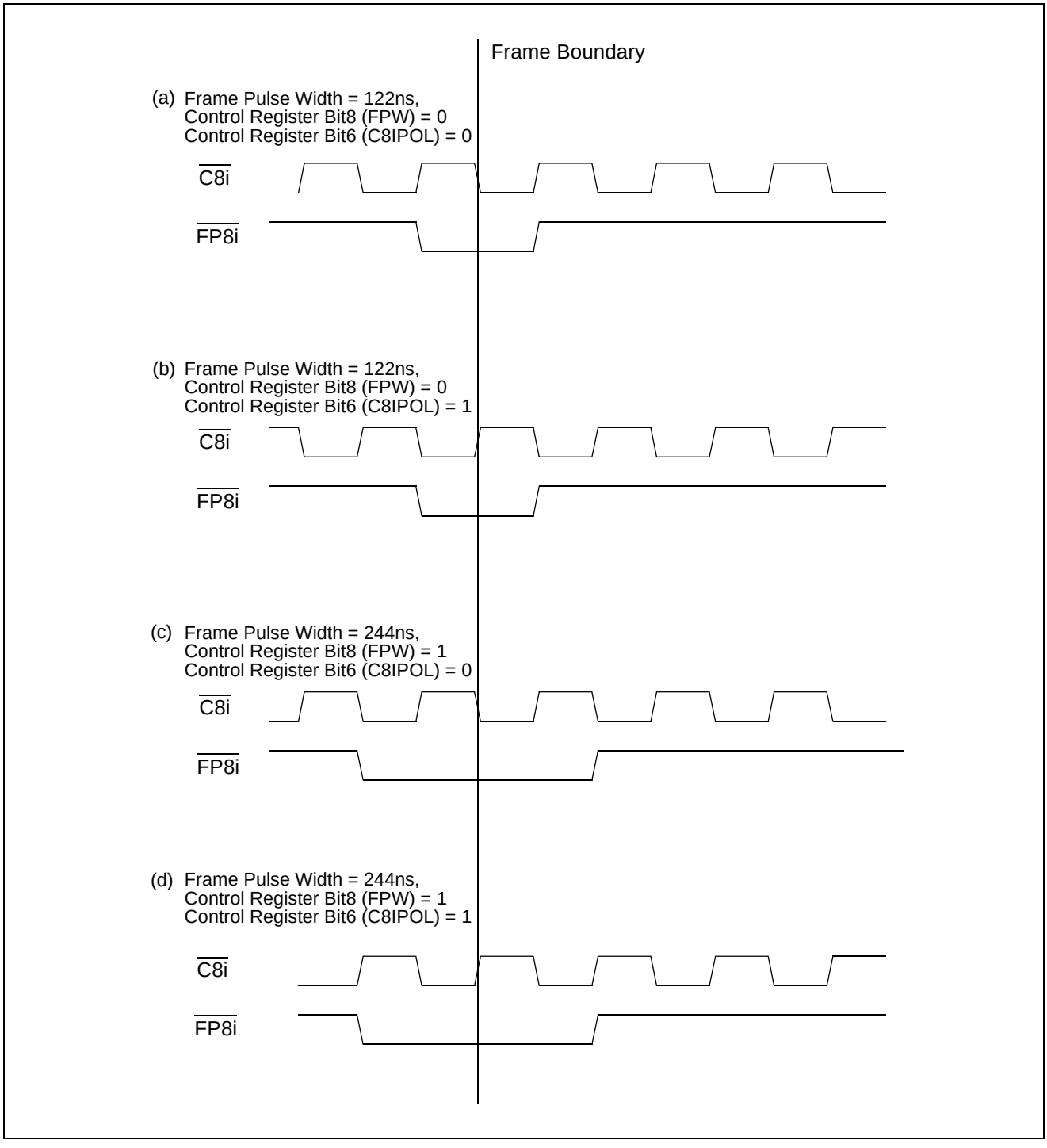


Figure 23 - Frame Boundary Conditions, ST-BUS Operation

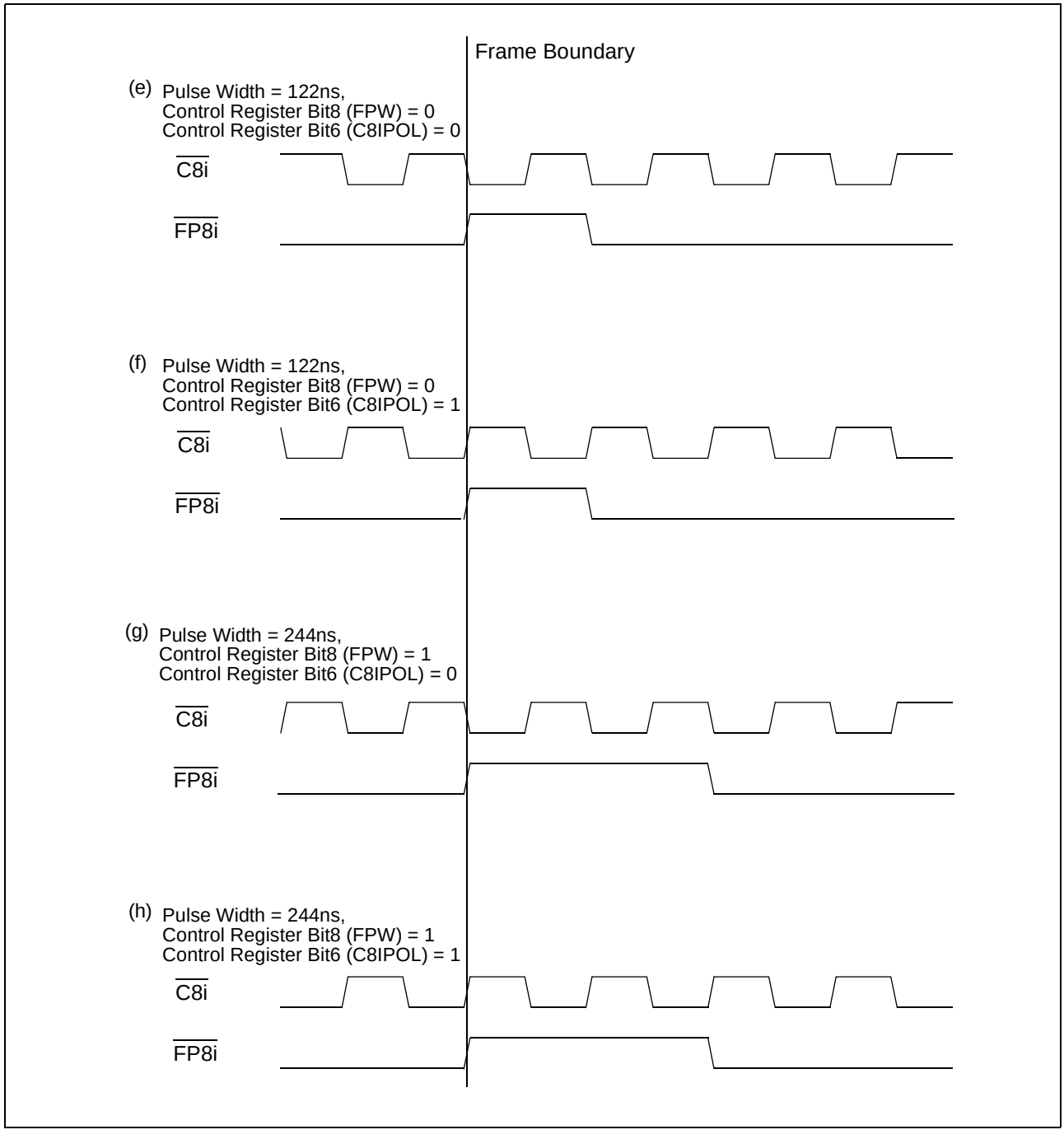


Figure 24 - Frame Boundary Conditions, GCI-Bus Operation

14.2 Block Programming Register (BPR)

Address 0001_H.

The Block Programming Register stores the bit patterns to be loaded into the connection memories when the Memory Block Programming feature is enabled. The BPE, LBPD[2:0] and BBPD[2:0] bits in the BPR register must be defined in the same write operation.

The BPE bit is set HIGH to commence the block programming operation. Programming is completed in one frame period and may be initiated at any time within a frame. The BPE bit returns to LOW to indicate that the block programming function has completed.

When BPE is HIGH, no other bits of the BPR register may be changed for at least a single frame period, except to abort the programming operation. The programming operation may be aborted by setting either BPE to LOW, or the Control Register bit, MBP, to LOW.

The **BPR** register is configured as follows.

Bit	Name	Reset Value	Description
15:7	Reserved	0	**Reserved** Must be set to 0 for normal operation
6:4	BBPD[2:0]	0	**Backplane Block Programming Data** These bits refer to the value loaded into the Backplane Connection Memory (BCM) when the Memory Block Programming feature is activated. When the MBP bit in the Control Register (CR) is set HIGH and BPE (in this register) is set HIGH, the contents of bits BBPD[2:0] are loaded into bits 15-13, respectively, of the BCM. Bits 12-0 of the BCM are set LOW.
3:1	LBPD[2:0]	0	**Local Block Programming Data** These bits refer to the value loaded into the Local Connection Memory (LCM), when the Memory Block Programming feature is activated. When the MBP bit in the Control Register is set HIGH and BPE (in this register) is set HIGH, the contents of bits LBPD[2:0] are loaded into bits 15-13, respectively, of the LCM. Bits 12-0 of the LCM are set LOW.
0	BPE	0	**Block Programming Enable** A LOW to HIGH transition of this bit enables the Memory Block Programming function. A LOW will be returned after 125 µs, upon completion of programming. Set LOW to abort the programming operation.

Table 20 - Block Programming Register Bits

14.3 Bit Error Rate Test Control Register (BERCR)

Address 0002_H.

The BER Test Control Register controls Backplane and Local port BER testing. It independently enables and disables transmission and reception. It is configured as follows:

Bit	Name	Reset Value	Description
15:12	Reserved	0	**Reserved** Must be set to 0 for normal operation
11	LOCKB	0	**Backplane Lock (READ ONLY)** This bit is automatically set HIGH when the receiver has locked to the incoming data sequence. The bit is reset by a LOW to HIGH transition on SBERRXB.
10	PRSTB	0	**PBER Reset for Backplane** A LOW to HIGH transition initializes the Backplane BER generator to the seed value.
9	CBERB	0	**Clear Bit Error Rate Register for Backplane** A LOW to HIGH transition in this bit resets the Backplane internal bit error counter and the Backplane Bit Error Register (BBERR) to zero.
8	SBERRXB	0	**Start Bit Error Rate Receiver for Backplane** A LOW to HIGH transition enables the Backplane BER receiver. The receiver monitors incoming data for reception of the seed value. When detected, the LOCK state is indicated (LOCKB), the receiver compares the incoming bits with the reference generator for bit equality, and increments the Backplane Bit Error Register (BBCR) on each failure. When LOW, bit comparison is disabled and the error count is frozen.
7	SBERTXB	0	**Start Bit Error Rate Transmitter for Backplane** A LOW to HIGH transition starts the BER transmission on the Backplane. When LOW, Backplane transmission is disabled.
6	PRBSB	0	**BER Mode Select for Backplane** When HIGH, a PRBS sequence of length 2^{23}-1 is selected for the Backplane port. When LOW, a PRBS sequence of length 2^{15}-1 is selected for the Backplane port.
5	LOCKL	0	**Local Lock (READ ONLY)** This bit is automatically set HIGH when the receiver has locked to the incoming data sequence. The bit is reset by a LOW to HIGH transition on SBERRXL
4	PRSTL	0	**PBER Reset for Local** A LOW to HIGH transition initializes the Local BER generator to the seed value.
3	CBERL	0	**Clear Bit Error Rate Register for Local** A LOW to HIGH transition resets the Local internal bit error counter and the Local Bit Error Register (LBERR) to zero.

Table 21 - Bit Error Rate Test Control Register (BERCR) Bits

Bit	Name	Reset Value	Description
2	SBERRXL	0	**Start Bit Error Rate Receiver for Local** A LOW to HIGH transition enables the Local BER receiver. The receiver monitors incoming data for reception of the seed value. When detected, the LOCK state is indicated (LOCKL), the receiver compares the incoming bits with the reference generator for bit equality, and increments the Local Bit Error Register (LBCR) on each failure. When LOW, bit comparison is disabled and the error count is frozen.
1	SBERTXL	0	**Start Bit Error Rate Transmitter for Local** A LOW to HIGH transition enables the Local BER transmission. When LOW, Local transmission is disabled.
0	PRBSL	0	**BER Mode Select for Local** When HIGH, a PRBS sequence of length 2^{23}-1 is selected for the Local port. When LOW, a PRBS sequence of length 2^{15}-1 is selected for the Local port.

Table 21 - Bit Error Rate Test Control Register (BERCR) Bits (continued)

14.4 Local Input Channel Delay Registers (LCDR0 to LCDR31)

Addresses 0003h to 0022_H.

Thirty-two Local Input Channel Delay Registers (LCDR0 to LCDR31) allow users to program the input channel delay for the Local input data streams LSTi0-31. The maximum possible adjustment is 511 channels and the **LCDR0 to LCDR31** registers are configured as follows:

LCDRn Bit (where n = 0 to 31 for Local Non-32Mbps Mode, n = 0 to 15 for Local 32Mbps Mode)	Name	Reset Value	Description
15:9	Reserved	0	**Reserved** Must be set to 0 for normal operation
8:0	LCD[8:0]	0	**Local Channel Delay Register** The binary value of these bits refers to the channel delay value for the Local input stream.

Table 22 - Local Input Channel Delay Register (LCDRn) Bits

14.4.1 Local Channel Delay Bits 8-0 (LCD8 - LCD0)

These nine bits define the delay, in channel numbers, the serial interface receiver takes to store the channel data from the Local input pins. The input channel delay can be selected to be up to 511 (32 Mbps streams), 255 (16 Mbps streams), 127 (8 Mbps streams), 63 (4 Mbps streams) or 31 (2 Mbps streams) channels from the frame boundary.

Input Stream Channel Delay	Corresponding Delay Bits LCD8-LCD0
0 Channel (Default)	0 0000 0000
1 Channel	0 0000 0001
2 Channels	0 0000 0010
3 Channels	0 0000 0011
4 Channels	0 0000 0100
5 Channels	0 0000 0101
...	...
509 Channels	1 1111 1101
510 Channels	1 1111 1110
511 Channels	1 1111 1111

Table 23 - Local Input Channel Delay (LCD) Programming Table

14.5 Local Input Bit Delay Registers (LIDR0 to LIDR31)

Addresses 0023_H to 0042_H.

There are thirty-two Local Input Delay Registers (LIDR0 to LIDR31).

When the SMPL_MODE bit in the Control Register is LOW, the input data sampling point defaults to the 3/4 bit location and LIDR0 to LIDR31 define the input bit and fractional bit delay of each Local stream. The possible bit delay adjustment is up to $7^3/_4$ bits, in steps of $^1/_4$ bit.

When the SMPL_MODE bit is HIGH, LIDR0 to LIDR31 define the input bit sampling point as well as the integer bit delay of each Local stream. The input bit sampling point can be adjusted in 1/4 bit increments. The bit delay can be adjusted in 1-bit increments from 0 to 7 bits.

The **LIDR0 to LIDR31** registers are configured as follows:

LIDRn Bit (where n = 0 to 31 for Local Non-32 Mbps Mode, n = 0 to 15 for Local 32Mbps Mode)	**Name**	**Reset Value**	**Description**
15:5	Reserved	0	**Reserved** Must be set to 0 for normal operation
4:0	LID[4:0]	0	**Local Input Bit Delay Register** When SMPL_MODE = LOW, the binary value of these bits refers to the input bit and fractional bit delay value (0 to $7^3/_4$). When SMPL_MODE = HIGH, the binary value of LID[1:0] refers to the input bit sampling point ($^1/_4$ to $^4/_4$). LID[4:2] refer to the integer bit delay value (0 to 7 bits).

Table 24 - Local Input Bit Delay Register (LIDRn) Bits

14.5.1 Local Input Delay Bits 4-0 (LID[4:0])

When SMPL_MODE = LOW, these five bits define the amount of input bit delay adjustment that the receiver uses to sample each input. Input bit delay adjustment can range up to $7^3/_4$ bit periods forward, with resolution of $^1/_4$ bit period. The default sampling point is at the $^3/_4$ bit location.

This can be described as: **no. of bits delay = LID[4:0] / 4**
For example, if LID[4:0] is set to 10011 (19), the input bit delay = 19 * $^1/_4$ = $4^3/_4$.

When SMPL_MODE = HIGH, the binary value of LID[1:0] refers to the input bit sampling point ($^1/_4$ to $^4/_4$). LID[4:2] refer to the integer bit delay value (0 to 7 bits). This means that bits can be delayed by an integer value of up to 7 and that the sampling point can vary from $^1/_4$ to $^4/_4$ in $^1/_4$-bit increments.

Table 25 illustrates the bit delay and sampling point selection.

LIDn					**SMPL_MODE = LOW**	**SMPL_MODE = HIGH**	
LID4	**LID3**	**LID2**	**LID1**	**LID0**	**Input Data Bit Delay**	**Input Data Bit Delay**	**Input Data Sampling Point**
0	0	0	0	0	0 (Default)	0 (Default)	3/4
0	0	0	0	1	1/4	0	4/4

Table 25 - Local Input Bit Delay and Sampling Point Programming Table

LIDn					SMPL_MODE = LOW	SMPL_MODE = HIGH	
LID4	LID3	LID2	LID1	LID0	Input Data Bit Delay	Input Data Bit Delay	Input Data Sampling Point
0	0	0	1	0	1/2	0	1/4
0	0	0	1	1	3/4	0	2/4
0	0	1	0	0	1	1	3/4
0	0	1	0	1	1 1/4	1	4/4
0	0	1	1	0	1 1/2	1	1/4
0	0	1	1	1	1 3/4	1	2/4
0	1	0	0	0	2	2	3/4
0	1	0	0	1	2 1/4	2	4/4
0	1	0	1	0	2 1/2	2	1/4
0	1	0	1	1	2 3/4	2	2/4
0	1	1	0	0	3	3	3/4
0	1	1	0	1	3 1/4	3	4/4
0	1	1	1	0	3 1/2	3	1/4
0	1	1	1	1	3 3/4	3	2/4
1	0	0	0	0	4	4	3/4
1	0	0	0	1	4 1/4	4	4/4
1	0	0	1	0	4 1/2	4	1/4
1	0	0	1	1	4 3/4	4	2/4
1	0	1	0	0	5	5	3/4
1	0	1	0	1	5 1/4	5	4/4
1	0	1	1	0	5 1/2	5	1/4
1	0	1	1	1	5 3/4	5	2/4
1	1	0	0	0	6	6	3/4
1	1	0	0	1	6 1/4	6	4/4
1	1	0	1	0	6 1/2	6	1/4
1	1	0	1	1	6 3/4	6	2/4
1	1	1	0	0	7	7	3/4
1	1	1	0	1	7 1/4	7	4/4
1	1	1	1	0	7 1/2	7	1/4
1	1	1	1	1	7 3/4	7	2/4

Table 25 - Local Input Bit Delay and Sampling Point Programming Table (continued)

14.6 Backplane Input Channel Delay Registers (BCDR0 to BCDR31)

Addresses 0043_H to 0062_H

Thirty-two Backplane Input Channel Delay Registers (BCDR0 to BCDR31) allow users to program the input channel delay for the Backplane input data streams BSTi0-31. The maximum possible adjustment is 511 channels and the **BCDR0 to BCDR31** registers are configured as follows:

BCDRn Bit (where n = 0 to 31 for Backplane Non-32 Mbps Mode, n = 0 to 15 for Backplane 32 Mbps Mode)	**Name**	**Reset Value**	**Description**
15:9	Reserved	0	**Reserved** Must be set to 0 for normal operation
8:0	BCD[8:0]	0	**Backplane Channel Delay Register** The binary value of these bits refers to the channel delay value for the Backplane input stream.

Table 26 - Backplane Input Channel Delay Register (BCDRn) Bits

14.6.1 Backplane Channel Delay Bits 8-0 (BCD8 - BCD0)

These nine bits define the delay, in channel numbers, the serial interface receiver takes to store the channel data from the Backplane input pins. The input channel delay can be selected to be up to 511 (32 Mbps streams), 255 (16 Mbps streams), 127 (8 Mbps streams), 63 (4 Mbps streams) or 31 (2 Mbps streams) channels from the frame boundary.

Input Stream Channel Delay	**Corresponding Delay Bits BCD8-BCD0**
0 Channel (Default)	0 0000 0000
1 Channel	0 0000 0001
2 Channels	0 0000 0010
3 Channels	0 0000 0011
4 Channels	0 0000 0100
5 Channels	0 0000 0101
...	...
509 Channels	1 1111 1101
510 Channels	1 1111 1110
511 Channels	1 1111 1111

Table 27 - Backplane Input Channel Delay (BCD) Programming Table

14.7 Backplane Input Bit Delay Registers (BIDR0 to BIDR31)

Addresses 0063_H to 0082_H

There are thirty-two Backplane Input Delay Registers (BIDR0 to BIDR31).

When the SMPL_MODE bit in the Control Register is LOW, the input data sampling point defaults to the 3/4 bit location and BIDR0 to BIDR31 define the input bit and fractional bit delay of each Backplane stream. The possible bit delay adjustment is up to $7^3/_4$ bits, in steps of $^1/_4$ bit.

When the SMPL_MODE bit is HIGH, BIDR0 to BIDR31 define the input bit sampling point as well as the integer bit delay of each Backplane stream. The input bit sampling point can be adjusted in 1/4 bit increments. The bit delay can be adjusted in 1-bit increments from 0 to 7 bits.

The **BIDR0 to BIDR31** registers are configured as follows:

BIDRn Bit (where n = 0 to 31 for Backplane Non-32 Mbps Mode, n = 0 to 15 for Backplane 32 Mbps Mode)	**Name**	**Reset Value**	**Description**
15:5	Reserved	0	**Reserved** Must be set to 0 for normal operation
4:0	BID[4:0]	0	**Backplane Input Bit Delay Register** When SMPL_MODE = LOW, the binary value of these bits refers to the input bit and fractional bit delay value (0 to $7^3/_4$). When SMPL_MODE = HIGH, the binary value of BID[1:0] refers to the input bit sampling point ($^1/_4$ to $^4/_4$). BID[4:2] refer to the integer bit delay value (0 to 7 bits).

Table 28 - Backplane Input Bit Delay Register (BIDRn) Bits

14.7.1 Backplane Input Delay Bits 4-0 (BID[4:0])

When SMPL_MODE = LOW, these five bits define the amount of input bit delay adjustment that the receiver uses to sample each input. Input bit delay adjustment can range up to $7^3/_4$ bit periods forward, with resolution of $^1/_4$ bit period. The default sampling point is at the $^3/_4$ bit location.

This can be described as: **no. of bits delay = BID[4:0] / 4**

For example, if BID[4:0] is set to 10011 (19), the input bit delay = 19 * $^1/_4$ = $4^3/_4$.

When SMPL_MODE = HIGH, the binary value of BID[1:0] refers to the input bit sampling point ($^1/_4$ to $^4/_4$). BID[4:2] refer to the integer bit delay value (0 to 7 bits). This means that bits can be delayed by an integer value of up to 7 and that the sampling point can vary from $^1/_4$ to $^4/_4$ in $^1/_4$-bit increments.

Table 29 illustrates the bit delay and sampling point selection.

BIDn					SMPL_MODE = LOW	SMPL_MODE = HIGH	
BID4	BID3	BID2	BID1	BID0	Input Data Bit Delay	Input Data Bit Delay	Input Data Sampling Point
0	0	0	0	0	0 (Default)	0 (Default)	3/4
0	0	0	0	1	1/4	0	4/4
0	0	0	1	0	1/2	0	1/4
0	0	0	1	1	3/4	0	2/4
0	0	1	0	0	1	1	3/4
0	0	1	0	1	1 1/4	1	4/4
0	0	1	1	0	1 1/2	1	1/4
0	0	1	1	1	1 3/4	1	2/4
0	1	0	0	0	2	2	3/4
0	1	0	0	1	2 1/4	2	4/4
0	1	0	1	0	2 1/2	2	1/4
0	1	0	1	1	2 3/4	2	2/4
0	1	1	0	0	3	3	3/4
0	1	1	0	1	3 1/4	3	4/4
0	1	1	1	0	3 1/2	3	1/4
0	1	1	1	1	3 3/4	3	2/4
1	0	0	0	0	4	4	3/4
1	0	0	0	1	4 1/4	4	4/4
1	0	0	1	0	4 1/2	4	1/4
1	0	0	1	1	4 3/4	4	2/4
1	0	1	0	0	5	5	3/4
1	0	1	0	1	5 1/4	5	4/4
1	0	1	1	0	5 1/2	5	1/4
1	0	1	1	1	5 3/4	5	2/4
1	1	0	0	0	6	6	3/4
1	1	0	0	1	6 1/4	6	4/4
1	1	0	1	0	6 1/2	6	1/4
1	1	0	1	1	6 3/4	6	2/4

Table 29 - Backplane Input Bit Delay and Sampling Point Programming Table

BIDn					SMPL_MODE = LOW	SMPL_MODE = HIGH	
BID4	BID3	BID2	BID1	BID0	Input Data Bit Delay	Input Data Bit Delay	Input Data Sampling Point
1	1	1	0	0	7	7	3/4
1	1	1	0	1	7 1/4	7	4/4
1	1	1	1	0	7 1/2	7	1/4
1	1	1	1	1	7 3/4	7	2/4

Table 29 - Backplane Input Bit Delay and Sampling Point Programming Table (continued)

14.8 Local Output Advancement Registers (LOAR0 to LOAR31)

Addresses 0083_H to $00A2_H$.

Thirty-two Local Output Advancement Registers (LOAR0 to LOAR31) allow users to program the output advancement for output data streams LSTo0 to LSTo31.

For 2 Mbps, 4 Mbps, 8 Mbps and 16 Mbps stream operation, the possible adjustment is -2 (15 ns), -4 (31 ns) or -6 (46 ns) cycles of the internal system clock (131.072 MHz).

For 32 Mbps stream operation, the possible adjustment is -1 (7.6 ns), -2 (15 ns) or -3 (23 ns) cycles of the internal system clock (131.072 MHz).

The **LOAR0** to **LOAR31** registers are configured as follows:

LOARn Bit (where n = 0 to 31 for Local Non-32 Mbps Mode, n = 0 to 15 for Local 32 Mbps Mode)	Name	Reset Value	Description
15:2	Reserved	0	**Reserved** Must be set to 0 for normal operation
1:0	LOA[1:0]	0	**Local Output Advancement Value**

Table 30 - Local Output Advancement Register (LOAR) Bits

14.8.1 Local Output Advancement Bits 1-0 (LOA1-LOA0)

The binary value of these two bits indicates the amount of offset that a particular stream output can be advanced with respect to the output frame boundary. When the advancement is 0, the serial output stream has the normal alignment with the generated frame pulse FP8o.

Local Output Advancement For 2 Mbps, 4 Mbps, 8 Mbps & 16 Mbps	Local Output Advancement For 32 Mbps	Corresponding Advancement Bits	
Clock Rate 131.072 MHz	Clock Rate 131.072 MHz	LOA1	LOA0
0 (Default)	0 (Default)	0	0
-2 cycles (~15 ns)	-1 cycle (~7.6 ns)	0	1

Table 31 - Local Output Advancement (LOAR) Programming Table

Local Output Advancement For 2 Mbps, 4 Mbps, 8 Mbps & 16 Mbps	Local Output Advancement For 32 Mbps	Corresponding Advancement Bits	
Clock Rate 131.072 MHz	**Clock Rate 131.072 MHz**	**LOA1**	**LOA0**
-4 cycles (~31 ns)	-2 cycles (~15 ns)	1	0
-6 cycles (~46 ns)	-3 cycles (~23 ns)	1	1

Table 31 - Local Output Advancement (LOAR) Programming Table (continued)

14.9 Backplane Output Advancement Registers (BOAR0 - BOAR31)

Addresses $00A3_H$ to $00C2_H$

Thirty-two Backplane Output Advancement Registers (BOAR0 to BOAR31) allow users to program the output advancement for output data streams BSTo0 to BSTo31.

For 2 Mbps, 4 Mbps, 8 Mbps and 16 Mbps stream operation, the possible adjustment is -2 (15 ns), -4 (31 ns) or -6 (46 ns) cycles of the internal system clock (131.072 MHz).

For 32 Mbps stream operation, the possible adjustment is -1 (7.6 ns), -2 (15 ns) or -3 (23 ns) cycles of the internal system clock (131.072 MHz).

The **BOAR0** to **BOAR31** registers are configured as follows:

BOARn Bit (where n = 0 to 31 for Backplane Non-32 Mbps Mode, n = 0 to 15 for Backplane 32 Mbps Mode)	**Name**	**Reset Value**	**Description**
15:2	Reserved	0	**Reserved** Must be set to 0 for normal operation
1:0	BOA[1:0]	0	**Backplane Output Advancement Value**

Table 32 - Backplane Output Advancement Register (BOAR) Bits

14.9.1 Backplane Output Advancement Bits 1-0 (BOA1-BOA0)

The binary value of these two bits indicates the amount of offset that a particular stream output can be advanced with respect to the output frame boundary. When the advancement is 0, the serial output stream has the normal alignment with the generated frame pulse $\overline{FP8o}$.

Backplane Output Advancement For 2 Mbps, 4 Mbps, 8 Mbps & 16 Mbps	Backplane Output Advancement For 32 Mbps	Corresponding Advancement Bits	
Clock Rate 131.072 MHz	**Clock Rate 131.072 MHz**	**BOA1**	**BOA0**
0 (Default)	0 (Default)	0	0
-2 cycles (~15 ns)	-1 cycle (~7.6 ns)	0	1
-4 cycles (~31 ns)	-2 cycles (~15 ns)	1	0
-6 cycles (~46 ns)	-3 cycles (~23 ns)	1	1

Table 33 - Backplane Output Advancement (BOAR) Programming Table

14.10 Local Bit Error Rate (BER) Registers

14.10.1 Local BER Start Send Register (LBSSR)

Address $00C3_H$.

The Local BER Start Send Register defines the output channel and the stream on which the BER sequence starts to be transmitted. The LBSSR register is configured differently for Non-32 Mbps and 32 Mbps Modes:

Bit	Name	Reset Value	Description
15:13	Reserved	0	**Reserved** Must be set to 0 for normal operation
12:8	LBSSA[4:0]	0	**Local BER Send Stream Address Bits** The binary value of these bits refers to the Local output stream which carries the BER data.
7:0	LBSCA[7:0]	0	**Local BER Send Channel Address Bits** The binary value of these bits refers to the Local output channel at which the BER data starts to be sent.

Table 34 - Local BER Start Send Register (LBSSR) Bits in Non-32 Mbps Mode

Bit	Name	Reset Value	Description
15:13	Reserved	0	**Reserved** Must be set to 0 for normal operation
12:9	LBSSA[3:0]	0	**Local BER Send Stream Address Bits** The binary value of these bits refers to the Local output stream which carries the BER data.
8:0	LBSCA[8:0]	0	**Local BER Send Channel Address Bits** The binary value of these bits refers to the Local output channel at which the BER data starts to be sent.

Table 35 - Local BER Start Send Register (LBSSR) Bits in 32 Mbps Mode

14.10.2 Local Transmit BER Length Register (LTXBLR)

Address $00C4_H$.

Local BER Transmit Length Register (**LTXBLR**) defines how many channels of the BER sequence will be transmitted during each frame. The minimum length of the BER transmitter is 1 channel. To set a desired BER length, set LTXBL8-0 bits for the desired length - 1 channel. For example, to run a BER test for 32 consecutive channels, program LTXBL to 000011111_B. The **LTXBLR** register is configured as follows:

Bit	Name	Reset Value	Description
15:9	Reserved	0	**Reserved** Must be set to 0 for normal operation
8:0	LTXBL[8:0]	0	**Local Transmit BER Length Bits** The binary value of these bits defines the number of channels in addition to the Start Channel allocated for the BER Transmitter. (i.e. Total Channels = LTXBL value + 1)

Table 36 - Local BER Length Register (LTXBLR) Bits

14.10.3 Local Receive BER Length Register (LRXBLR)

Address $00C5_H$.

Local BER Receive Length Register (**LRXBLR**) defines how many channels of the BER sequence will be received during each frame. The minimum length of the BER receiver is 1 channel. To set a desired BER length, set LRXBL8-0 bits for the desired length - 1 channel. For example, to receive a BER test for 32 consecutive channels, program LRXBL to 000011111_B. The **LRXBLR** register is configured as follows:

Bit	Name	Reset Value	Description
15:9	Reserved	0	**Reserved** Must be set to 0 for normal operation
8:0	LRXBL[8:0]	0	**Local Receive BER Length Bits** The binary value of these bits defines the number of channels in addition to the Start Channel allocated for the BER Receiver. (i.e., Total Channels = LRXBL value + 1)

Table 37 - Local Receive BER Length Register (LRXBLR) Bits

14.10.4 Local BER Start Receive Register (LBSRR)

Address $00C6_H$.

Local BER Start Receive Register defines the input stream and start channel at which the BER sequence shall start to be received. The **LBSRR** register is configured differently for Non-32 Mbps and 32 Mbps Modes:

Bit	Name	Reset Value	Description
15:13	Reserved	0	**Reserved** Must be set to 0 for normal operation
12:8	LBRSA[4:0]	0	**Local BER Receive Stream Address Bits** The binary value of these bits refers to the Local input stream configured to receive the BER data.
7:0	LBRCA[7:0]	0	**Local BER Receive Channel Address Bits** The binary value of these bits refers to the Local input channel at which the BER data starts to be compared.

Table 38 - Local BER Start Receive Register (LBSRR) Bits for Non-32 Mbps Mode

Bit	Name	Reset Value	Description
15:13	Reserved	0	**Reserved** Must be set to 0 for normal operation
12:9	LBRSA[3:0]	0	**Local BER Receive Stream Address Bits** The binary value of these bits refers to the Local input stream configured to receive the BER data.
8:0	LBRCA[8:0]	0	**Local BER Receive Channel Address Bits** The binary value of these bits refers to the Local input channel at which the BER data starts to be compared.

Table 39 - Local BER Start Receive Register (LBSRR) Bits for 32 Mbps Mode

14.10.5 Local BER Count Register (LBCR)

Address $00C7_H$.

Local BER Count Register contains the number of counted errors. This register is read-only. The **LBCR** register is configured as follows:

Bit	Name	Reset Value	Description
15:0	LBC[15:0]	0	**Local Bit Error Rate Count** The binary value of the bits defines the Local Bit Error count. If the number of errors exceeds the maximum counter value, this counter will stay at $FFFF_H$ until the CBERL bit in the BERCR register clears it.

Table 40 - Local BER Count Register (LBCR) Bits

14.11 Backplane Bit Error Rate (BER) Registers

14.11.1 Backplane BER Start Send Register (BBSSR)

Address $00C8_H$.

Backplane BER Start Send Register defines the output channel and the stream on which the BER sequence is transmitted.

The **BBSSR** register is configured as follows:

Bit	Name	Reset Value	Description
15:14	Reserved	0	**Reserved** Must be set to 0 for normal operation
13:9	BBSSA[4:0]	0	**Backplane BER Send Stream Address Bits** The binary value of these bits refers to the Backplane output stream which carries the BER data.
8:0	BBSCA[8:0]	0	**Backplane BER Send Channel Address Bits** The binary value of these bits refers to the Backplane output channel at which the BER data starts to be sent.

Table 41 - Backplane BER Start Send Register (BBSSR) Bits

14.11.2 Backplane Transmit BER Length Register (BTXBLR)

Address $00C9_H$.

Backplane Transmit BER Length Register (**BTXBLR**) defines how many channels of the BER sequence will be transmitted in each frame. The minimum length of the BER transmitter is 1 channel. To set a desired BER length, set BTXBL8-0 bits for the desired length - 1 channel. For example, to run a BER test for 32 consecutive channels, program BTXBL to 000011111_B. The **BTXBLR** register is configured as follows:

Bit	Name	Reset Value	Description
15:9	Reserved	0	**Reserved** Must be set to 0 for normal operation
8:0	BTXBL[8:0]	0	**Backplane Transmit BER Length Bits** The binary value of these bits defines the number of channels in addition to the Start Channel allocated for the BER Transmitter. (i.e., Total Channels = BTXBL value + 1)

Table 42 - Backplane Transmit BER Length (BTXBLR) Bits

14.11.3 Backplane Receive BER Length Register (BRXBLR)

Address $00CA_H$.

Backplane Receive BER Length Register (**BRXBLR**) defines how many channels of the BER sequence will be received in each frame. The minimum length of the BER receiver is 1 channel. To set a desired BER length, set BRXBL8-0 bits for the desired length - 1 channel. For example, to receive a BER test for 32 consecutive channels, program BRXBL to 000011111_B. The **BRXBLR** register is configured as follows:

Bit	Name	Reset Value	Description
15:9	Reserved	0	**Reserved** Must be set to 0 for normal operation
8:0	BRXBL[8:0]	0	**Backplane Receive BER Length Bits** The binary value of these bits defines the number of channels in addition to the Start Channel allocated for the BER Receiver. (i.e. Total Channels = BRXBL value + 1)

Table 43 - Backplane Receive BER Length (BRXBLR) Bits

14.11.4 Backplane BER Start Receive Register (BBSRR)

Address $00CB_H$.

Backplane BER Start Receive Register defines the input stream and the start channel at which the BER sequence shall start to be received. The **BBSRR** register is configured as follows:

Bit	Name	Reset Value	Description
15:14	Reserved	0	**Reserved** Must be set to 0 for normal operation
13:9	BBRSA[4:0]	0	**Backplane BER Receive Stream Address Bits** The binary value of these bits refers to the Backplane input stream configured to receive the BER data.
8:0	BBRCA[8:0]	0	**Backplane BER Receive Channel Address Bits** The binary value of these bits refers to the Backplane input channel at which the BER data starts to be compared.

Table 44 - Backplane BER Start Receive Register (BBSRR) Bits

14.11.5 Backplane BER Count Register (BBCR)

Address $00CC_H$.

Backplane BER Count Register contains the number of counted errors. This register is read-only.

The **BBCR** register is configured as follows:

Bit	Name	Reset Value	Description
15:0	BBC[15:0]	0	**Backplane Bit Error Rate Count** The binary value of these bits defines the Backplane Bit Error count. If the number of errors exceeds the maximum counter value, this counter will stay at $FFFF_H$ until the CBERB bit in the BERCR register clears it.

Table 45 - Backplane BER Count Register (BBCR) Bits

14.12 Local Bit Rate Registers

14.12.1 Local Input Bit Rate Registers (LIBRR0 - LIBRR31)

Addresses $00CD_H$ to $00EC_H$.

Thirty-two Local Input Bit Rate Registers allow the bit rate for each individual stream to be set to 2, 4, 8 or 16 Mbps. These registers may be overridden by setting Local 32 Mbps Mode in the Control Register (via the MODE32L bit), in which case, Local input streams 0-15 will operate at 32 Mbps and Local input streams 16-31 will be unused.

The **LIBRR** registers are configured as follows:

LIBRn (for n=0 to 31)	Name	Reset Value	Description
15:2	Reserved	0	**Reserved** Must be set to 0 for normal operation
1:0	LIBR[1:0]	0	**Local Input Bit Rate**

Table 46 - Local Input Bit Rate Register (LIBRR) Bits

MODE32L	LIBR1	LIBR0	Bit rate for stream n
0	0	0	2 Mbps
0	0	1	4 Mbps
0	1	0	8 Mbps
0	1	1	16 Mbps
1	X	X	32 Mbps

Table 47 - Local Input Bit Rate (LIBR) Programming Table

14.12.2 Local Output Bit Rate Registers (LOBRR0 - LOBRR31)

Addresses $00ED_H$ to $010C_H$.

Thirty-two Local Output Bit Rate Registers allow the bit rate for each individual stream to be set to 2, 4, 8 or 16 Mbps. These registers may be overridden by setting Local 32 Mbps Mode in the Control Register (via the MODE32L bit), in which case, Local output streams 0-15 will operate at 32 Mbps and Local output streams 16-31 will be unused. The **LOBRR** registers are configured as follows:

LOBRn Bit (where n = 0 to 31)	**Name**	**Reset Value**	**Description**
15:2	Reserved	0	**Reserved** Must be set to 0 for normal operation
1:0	LOBR[1:0]	0	**Local Output Bit Rate**

Table 48 - Local Output Bit Rate Register (LOBRR) Bits

MODE32L	**LOBR1**	**LOBR0**	**Bit rate for stream n**
0	0	0	2 Mbps
0	0	1	4 Mbps
0	1	0	8 Mbps
0	1	1	16 Mbps
1	X	X	32 Mbps

Table 49 - Local Output Bit Rate (LOBR) Programming Table

14.13 Backplane Bit Rate Registers

14.13.1 Backplane Input Bit Rate Registers (BIBRR0 - BIBRR31)

Addresses $010D_H$ to $012C_H$.

Thirty-two Backplane Input Bit Rate Registers allow the bit rate for each individual stream to be set to 2, 4, 8 or 16 Mbps. These registers may be overridden by setting Backplane 32 Mbps Mode in the Control Register (via the MODE32B bit), in which case, Backplane input streams 0-15 will operate at 32 Mbps and Backplane input streams 16-31 will be unused.

The **BIBRR** registers are configured as follows:

BIBRn Bit (for n = 0 to 31)	**Name**	**Reset Value**	**Description**
15:2	Reserved	0	**Reserved** Must be set to 0 for normal operation
1:0	BIBR[1:0]	0	**Backplane Input Bit Rate**

Table 50 - Backplane Input Bit Rate Register (BIBRR) Bits

MODE32B	BIBR1	BIBR0	Bit rate for stream n
0	0	0	2 Mbps
0	0	1	4 Mbps
0	1	0	8 Mbps
0	1	1	16 Mbps
1	X	X	32 Mbps

Table 51 - Backplane Input Bit Rate (BIBR) Programming Table

14.13.2 Backplane Output Bit Rate Registers (BOBRR0 - BOBRR31)

Addresses $012D_H$ to $014C_H$.

Thirty-two Backplane Output Bit Rate Registers allow the bit rate for each individual stream to be set to 2, 4, 8 or 16 Mbps. These registers may be overridden by setting Backplane 32 Mbps Mode in the Control Register (via the MODE32B bit), in which case, Backplane output streams 0-15 will operate at 32 Mbps and Backplane output streams 16-31 will be unused. The **BOBRR** registers are configured as follows:

BOBRn Bit (for n = 0 to 31)	Name	Reset Value	Description
15:2	Reserved	0	**Reserved** Must be set to 0 for normal operation
1:0	BOBR[1:0]	0	**Backplane Output Bit Rate**

Table 52 - Backplane Output Bit Rate Register (BOBRR) Bits

MODE32B	BOBR1	BOBR0	Bit rate for stream n
0	0	0	2 Mbps
0	0	1	4 Mbps
0	1	0	8 Mbps
0	1	1	16 Mbps
1	X	X	32 Mbps

Table 53 - Backplane Output Bit Rate (BOBRR) Programming Table

14.14 Memory BIST Register

Address $014D_H$.

The Memory BIST Register enables the self-test of chip memory. Two consecutive write operations are required to start MBIST: the first with only Bit 12 (LV_TM) set HIGH (i.e., 1000h); the second with Bit 12 maintained HIGH but with the required start bit(s) also set HIGH.

The **MBISTR** register is configured as follows:

Bit	Name	Reset Value	Description
15:13	Reserved	0	**Reserved** Must be set to 0 for normal operation
12	LV_TM	0	**MBIST Test Enable** Set HIGH to enable MBIST mode. Set LOW for normal operation.
11	BISTSDB	0	**Backplane Data Memory Start BIST Sequence** Sequence enabled on LOW to HIGH transition.
10	BISTCDB	0	**Backplane Data Memory BIST Sequence Completed (Read-only)** This bit must be polled - when HIGH, indicates completion of Backplane Data Memory BIST sequence.
9	BISTPDB	0	**Backplane Data Memory Pass/Fail Bit (Read-only)** This bit indicates the Pass/Fail status following completion of the Backplane Data Memory BIST sequence (indicated by assertion of BISTCDB). A HIGH indicates Pass, a LOW indicates Fail.
8	BISTSDL	0	**Local Data Memory Start BIST Sequence** Sequence enabled on LOW to HIGH transition.
7	BISTCDL	0	**Local Data Memory BIST Sequence Completed (Read-only)** This bit must be polled - when HIGH, indicates completion of Local Data Memory BIST sequence.
6	BISTPDL	0	**Local Data Memory Pass/Fail Bit (Read-only)** This bit indicates the Pass/Fail status following completion of the Local Data Memory BIST sequence (indicated by assertion of BISTCDL). A HIGH indicates Pass, a LOW indicates Fail.
5	BISTSCB	0	**Backplane Connection Memory Start BIST Sequence** Sequence enabled on LOW to HIGH transition.
4	BISTCCB	0	**Backplane Connection Memory BIST Sequence Completed (Read-only)** This bit must be polled - when HIGH, indicates completion of Backplane Connection Memory BIST sequence.
3	BISTPCB	0	**Backplane Connection Memory Pass/Fail Bit (Read-only)** This bit indicates the Pass/Fail status following completion of the Backplane Connection Memory BIST sequence (indicated by assertion of BISTCCB). A HIGH indicates Pass, a LOW indicates Fail.
2	BISTSCL	0	**Local Connection Memory Start BIST Sequence** Sequence enabled on LOW to HIGH transition.

Table 54 - Memory BIST Register (MBISTR) Bits

Bit	Name	Reset Value	Description
1	BISTCCL	0	**Local Connection Memory BIST Sequence Completed (Read-only)** This bit must be polled - when HIGH, indicates completion of Local Connection Memory BIST sequence.
0	BISTPCL	0	**Local Connection Memory Pass/Fail Bit (Read-only)** This bit indicates the Pass/Fail status following completion of the Local Connection Memory BIST sequence (indicated by assertion of BISTCCL). A HIGH indicates Pass, a LOW indicates Fail.

Table 54 - Memory BIST Register (MBISTR) Bits (continued)

14.15 Device Identification Register

Address $3FFF_H$.

The Device Identification Register stores the binary value of the silicon revision number and the Device ID. This register is read-only. The **DIR** register is configured as follows:

Bit	Name	Reset Value	Description
15:8	Reserved	0	**Reserved** Will read 0 in normal operation
7:4	RC[3:0]	0000	**Revision Control Bits**
3	Reserved	0	**Reserved** Will read 0 in normal operation
2:0	DID[2:0]	000	**Device ID**

Table 55 - Device Identification Register (DIR) Bits

15.0 DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Core Supply Voltage	V_{DD_CORE}	-0.5	2.5	V
2	I/O Supply Voltage	V_{DD_IO}	-0.5	5.0	V
3	PLL Supply Voltage	V_{DD_PLL}	-0.5	2.5	V
4	Input Voltage (non-5 V tolerant inputs)	V_I	-0.5	V_{DD_IO} +0.5	V
5	Input Voltage (5 V tolerant inputs)	V_{I_5V}	-0.5	7.0	V
6	Continuous Current at digital outputs	I_o		15	mA
7	Package power dissipation	P_D		1.5	W
8	Storage temperature	T_S	- 55	+125	°C

***** Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

	Characteristics	Sym.	Min.	Typ.	Max.	Units
1	Operating Temperature	T_{OP}	-40	25	+85	°C
2	Positive Supply	V_{DD_IO}	3.0	3.3	3.6	V
3	Positive Supply	V_{DD_CORE}	1.71	1.8	1.89	V
4	Positive Supply	V_{DD_PLL}	1.71	1.8	1.89	V
5	Input Voltage	V_I	0		V_{DD_IO}	V
6	Input Voltage on 5 V Tolerant Inputs	V_{I_5V}	0		5.5	V

Voltages are with respect to ground (V_{SS}) unless otherwise stated.

DC Electrical Parameters

		Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1a	I N P U T S	Supply Current	I_{DD_Core}			4	mA	Static I_{DD_Core} and PLL current
1b		Supply Current	I_{DD_Core}		240	290	mA	Applied clock C8i = 8.192 MHz
1c		Supply Current	I_{DD_IO}			100	µA	Static I_{DD_IO}
1d		Supply Current	I_{DD_IO}		14	18	mA	I_{AV} with all output streams at max. data rate unloaded
2		Input High Voltage	V_{IH}	2.0			V	
3		Input Low Voltage	V_{IL}			0.8	V	
4		Input Leakage (input pins) Input Leakage (bi-directional pins)	I_{IL} I_{BL}			5 5	µA µA	$0 < V < V_{DD\_IO}$ Note 1
		Weak Pullup Current	I_{PU}			200	µA	Input at 0V
5		Weak Pulldown Current	I_{PD}			200	µA	Input at V_{DD_IO}
6		Input Pin Capacitance	C_I			5	pF	
7	O U T P U T S	Output High Voltage	V_{OH}	2.4			V	I_{OH} = 8mA
8		Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8mA
9		High impedance Leakage	I_{OZ}			5	µA	$0 \leq V_0 \leq V_{DD\_IO}$ Note 1
10		Output Pin Capacitance	C_O			5	pF	

Voltages are with respect to ground (V_{SS}) unless otherwise stated.
Note 1: Maximum leakage on pins (output or I/O pins in high impedance state) is over an applied voltage (V)

16.0 AC Electrical Characteristics

AC Electrical Characteristics Timing Parameter Measurement: Voltage Levels

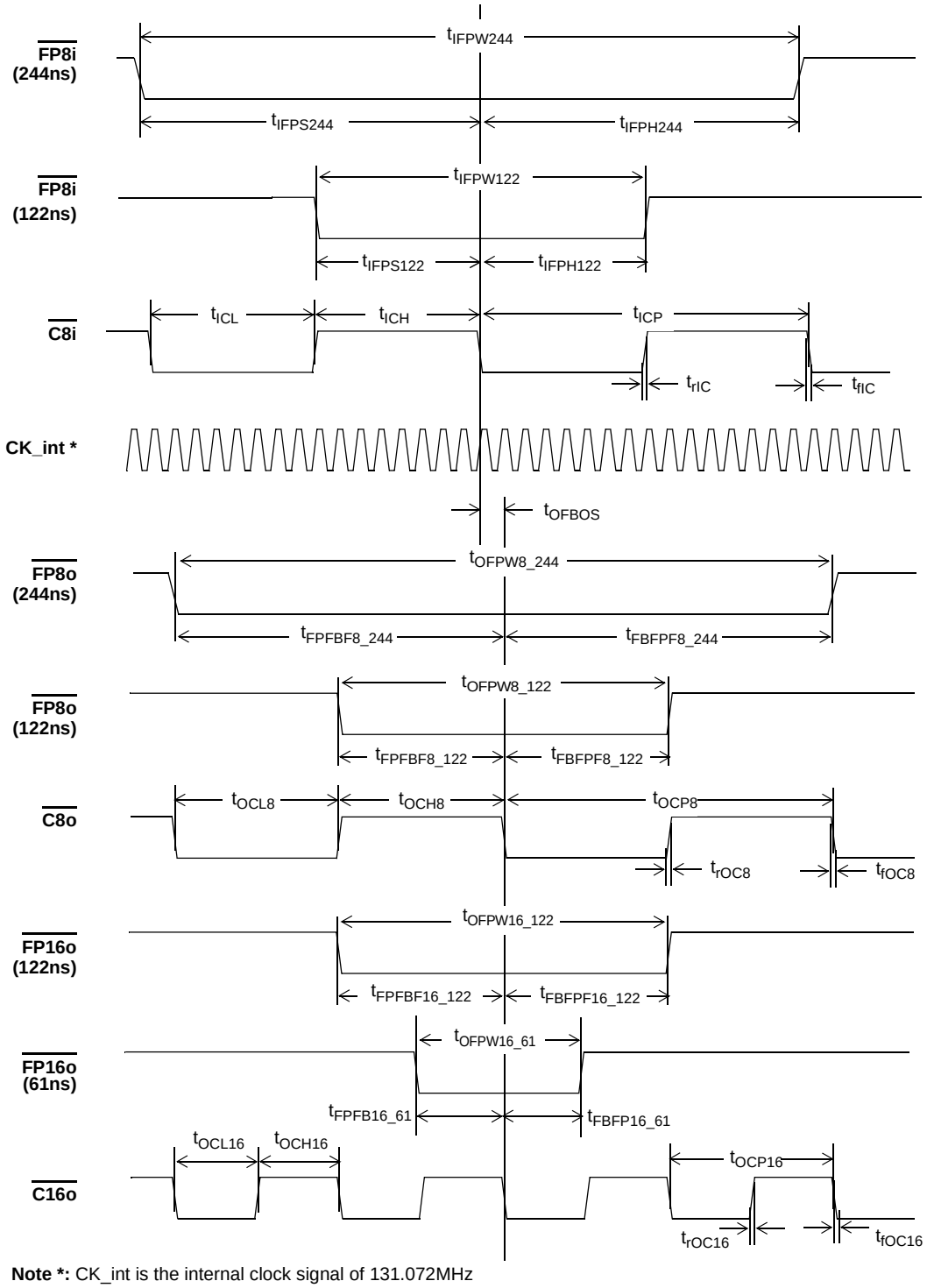
	Characteristics	Sym.	Level	Units	Conditions
1	CMOS Threshold	V_{CT}	$0.5V_{DD\_IO}$	V	$3.0V \leq V_{DD\_IO} \leq 3.6V$
2	Rise/Fall Threshold Voltage High	V_{HM}	$0.7V_{DD\_IO}$	V	$3.0V \leq V_{DD\_IO} \leq 3.6V$
3	Rise/Fall Threshold Voltage Low	V_{LM}	$0.3V_{DD\_IO}$	V	$3.0V \leq V_{DD\_IO} \leq 3.6V$

Input and Output Clock Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	$\overline{FP8i}$, Input Frame Pulse Width	$t_{IFPW244}$ $t_{IFPW122}$	210 10	244 122	350 220	ns	
2	Input Frame Pulse Setup Time (before $\overline{C8i}$ clock falling/rising edge)	$t_{IFPS244}$ $t_{IfPS122}$	5 5		110 60	ns	
3	Input Frame Pulse Hold Time (from $\overline{C8i}$ clock falling/rising edge)	$t_{IFPH244}$ $t_{IFPH122}$	0 0		110 60	ns	
4	$\overline{C8i}$ Clock Period (Average value, does not consider the effects of jitter)	t_{ICP}	120	122	124	ns	
5	$\overline{C8i}$ Clock Pulse Width High	t_{ICH}	50	61	70	ns	
6	$\overline{C8i}$ Clock Pulse Width Low	t_{ICL}	50	61	70	ns	
7	$\overline{C8i}$ Clock Rise/Fall Time	t_{rIC}, t_{fIC}	0	2	3	ns	
8	$\overline{C8i}$ Cycle to Cycle Variation (This values is with respect to the typical $\overline{C8i}$ Clock Period, and using mid-bit sampling)	t_{CCVIC}	-7.0 -8.5		7.0 8.5	ns ns	32Mbps 16Mbps or lower.
9	Output Frame Boundary Offset	t_{OFBOS}		7	9.5	ns	
10	$\overline{FP8o}$ Frame Pulse Width	t_{OFPW8_244} t_{OFPW8_122}	224 117	244 122	264 127	ns	FPW =1 FPW=0 C_L=60pF
11	$\overline{FP8o}$ Output Delay (from frame pulse edge to output frame boundary)	t_{FPFBF8_244} t_{FPFBF8_122}	117 58	122 61	127 64	ns	FPW =1 FPW=0 C_L=60pF
12	$\overline{FP8o}$ Output Delay (from output frame boundary to frame pulse edge)	t_{FBFPF8_244} t_{FBFPF8_122}	117 58	122 61	127 64	ns	FPW =1 FPW=0 C_L=60pF
13	$\overline{C8o}$ Clock Period	t_{OCP8}	117	122	127	ns	C_L=60pF
14	$\overline{C8o}$ Clock Pulse Width High	t_{OCH8}	58	61	64	ns	
15	$\overline{C8o}$ Clock Pulse Width Low	t_{OCL8}	58	61	64	ns	
16	$\overline{C8o}$ Clock Rise/Fall Time	t_{rOC8}, t_{fOC8}	3		7	ns	

Input and Output Clock Timing (continued)

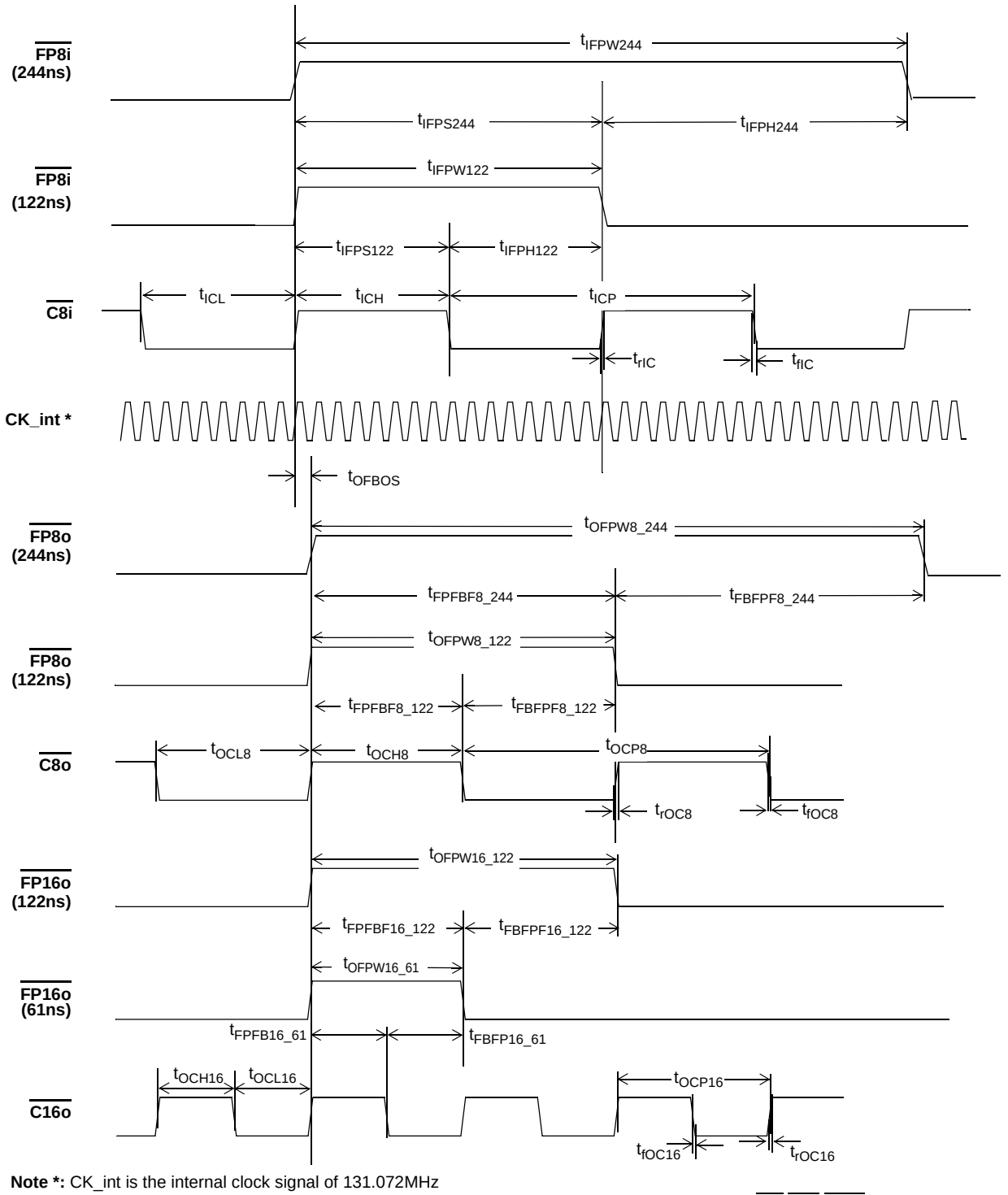
	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
17	$\overline{\text{FP16o}}$ Frame Pulse Width	t_{OFPW16_122} t_{OFPW16_61}	117 58	122 61	127 64	ns	FPW =1 FPW=0 C_L=60pF
18	$\overline{\text{FP16o}}$ Output Delay (from frame pulse edge to output frame boundary)	$t_{FPFBF16\_122}$ $t_{FPFBF16\_61}$	58 29	61 31	64 33	ns	FPW =1 FPW=0
19	$\overline{\text{FP16o}}$ Output Delay (from output frame boundary to frame pulse edge)	$t_{FBFPF16\_122}$ $t_{FBFPF16\_61}$	58 29	61 31	64 33	ns	FPW =1 FPW=0
20	$\overline{\text{C16o}}$ Clock Period	t_{OCP16}	58	61	64	ns	C_L=60pF
21	$\overline{\text{C16o}}$ Clock Pulse Width High	t_{OCH16}	29	31	33	ns	
22	$\overline{\text{C16o}}$ Clock Pulse Width Low	t_{OCL16}	29	31	33	ns	
23	$\overline{\text{C16o}}$ Clock Rise/Fall Time	t_{rOC16}, t_{fOC16}	3		7	ns	



Note *: CK_int is the internal clock signal of 131.072MHz

Note **: Although the figures above show the frame boundary as measured from the falling edge of C8i/C8o/C16o, the frame-controlling edge of C8i/C8o/C16o may be the rising edge, as configured via the C8iPOL and COPOL bits of the Control Register.

Figure 25 - Input and Output Clock Timing Diagram for ST-BUS



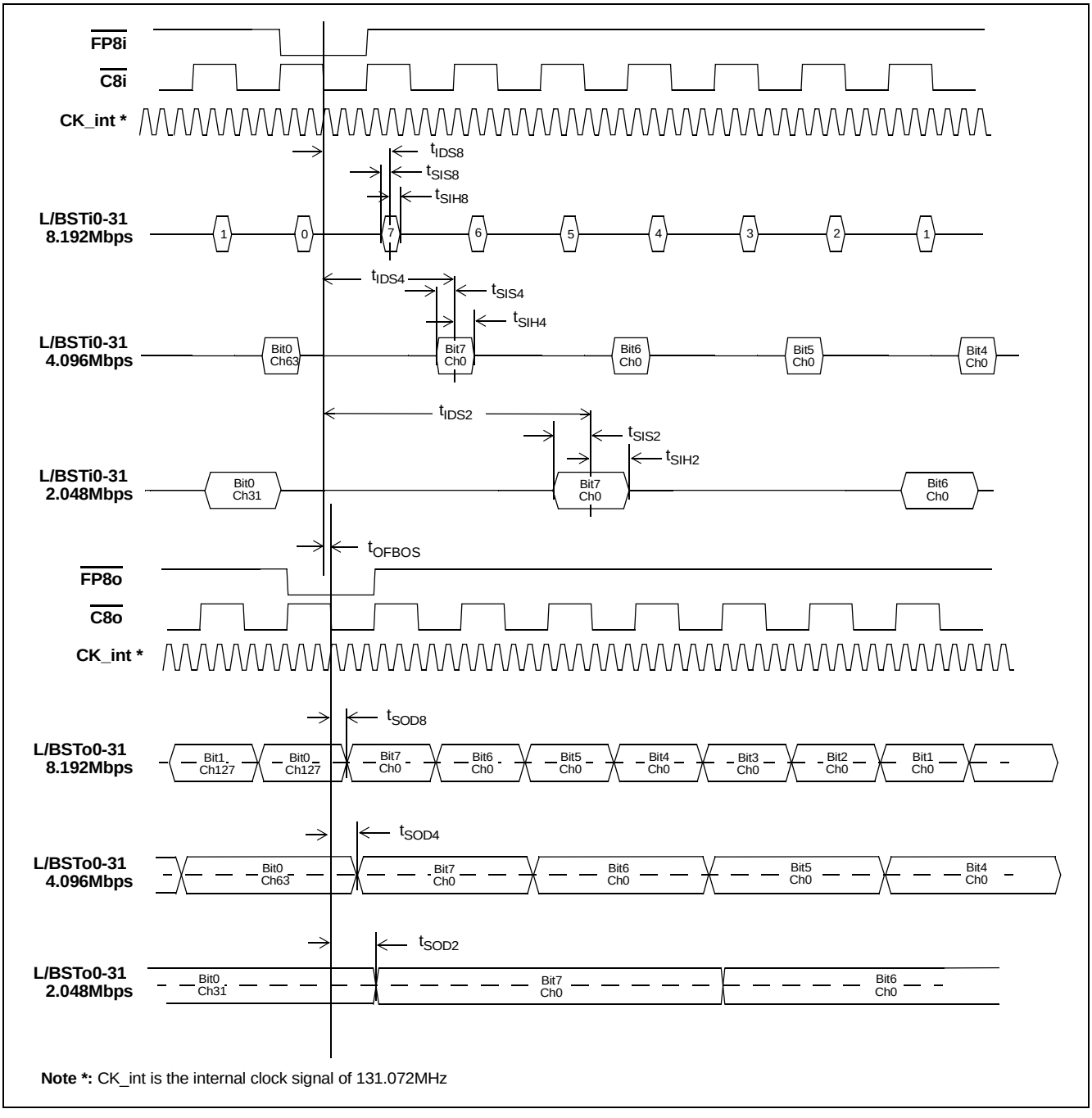
Note *: CK_int is the internal clock signal of 131.072MHz

Note **: Although the figures above show the frame boundary as measured from the rising edge of $\overline{C8i}$/$\overline{C8o}$/$\overline{C16o}$, the frame-controlling edge of $\overline{C8i}$/$\overline{C8o}$/$\overline{C16o}$ may be the rising edge, as configured via the C8iPOL and COPOL bits of the Control Register.

Figure 26 - Input and Output Clock Timing Diagram for GCI-Bus

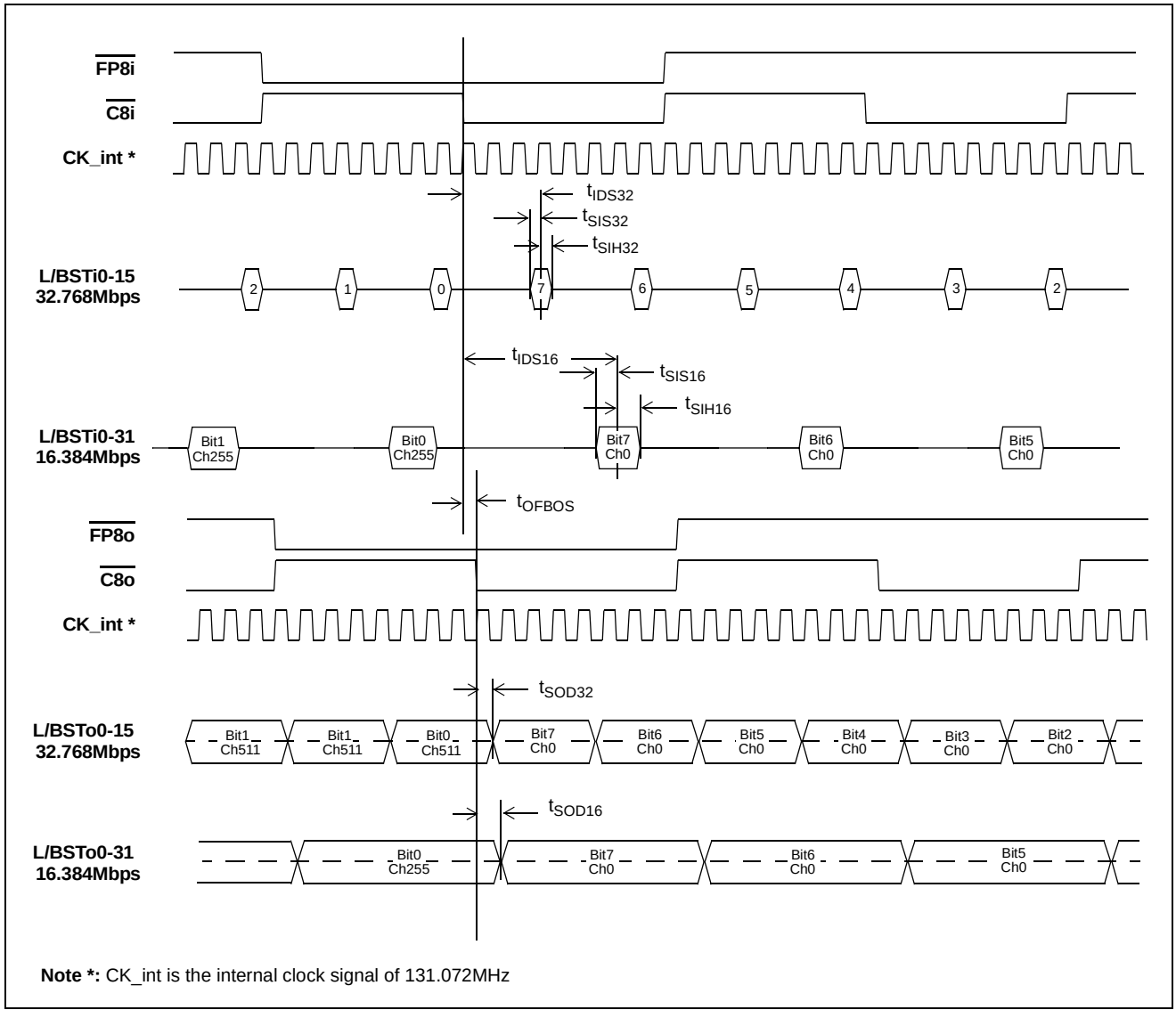
Local and Backplane Data Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	Local/Backplane Input Data Sampling Point	t_{IDS32} t_{IDS16} t_{IDS8} t_{IDS4} t_{IDS2}	20 43 87 178 357	23 46 92 183 366	26 49 97 188 375	ns	With SMPL_MODE = 0 (3/4-bit sampling) and zero offset.
2	Local/Backplane Serial Input Set-up Time	t_{SIS32} t_{SIS16} t_{SIS8} t_{SIS4} t_{SIS2}	2 2 2 2 2			ns	With respect to **Min**. Input Data Sampling Point
3	Local/Backplane Serial Input Hold Time	t_{SIH32} t_{SIH16} t_{SIH8} t_{SIH4} t_{SIH2}	2 2 2 2 2			ns	With respect to **Max**. Input Data Sampling Point
4	Output Frame Boundary Offset	t_{OFBOS}		7	9.5	ns	
5	Local/Backplane Serial Output Delay	t_{SOD32} t_{SOD16} t_{SOD8} t_{SOD4} t_{SOD2}			4.5 4.5 4.5 4.5 4.5	ns	C_L=50pF These numbers are referencing output frame boundary.



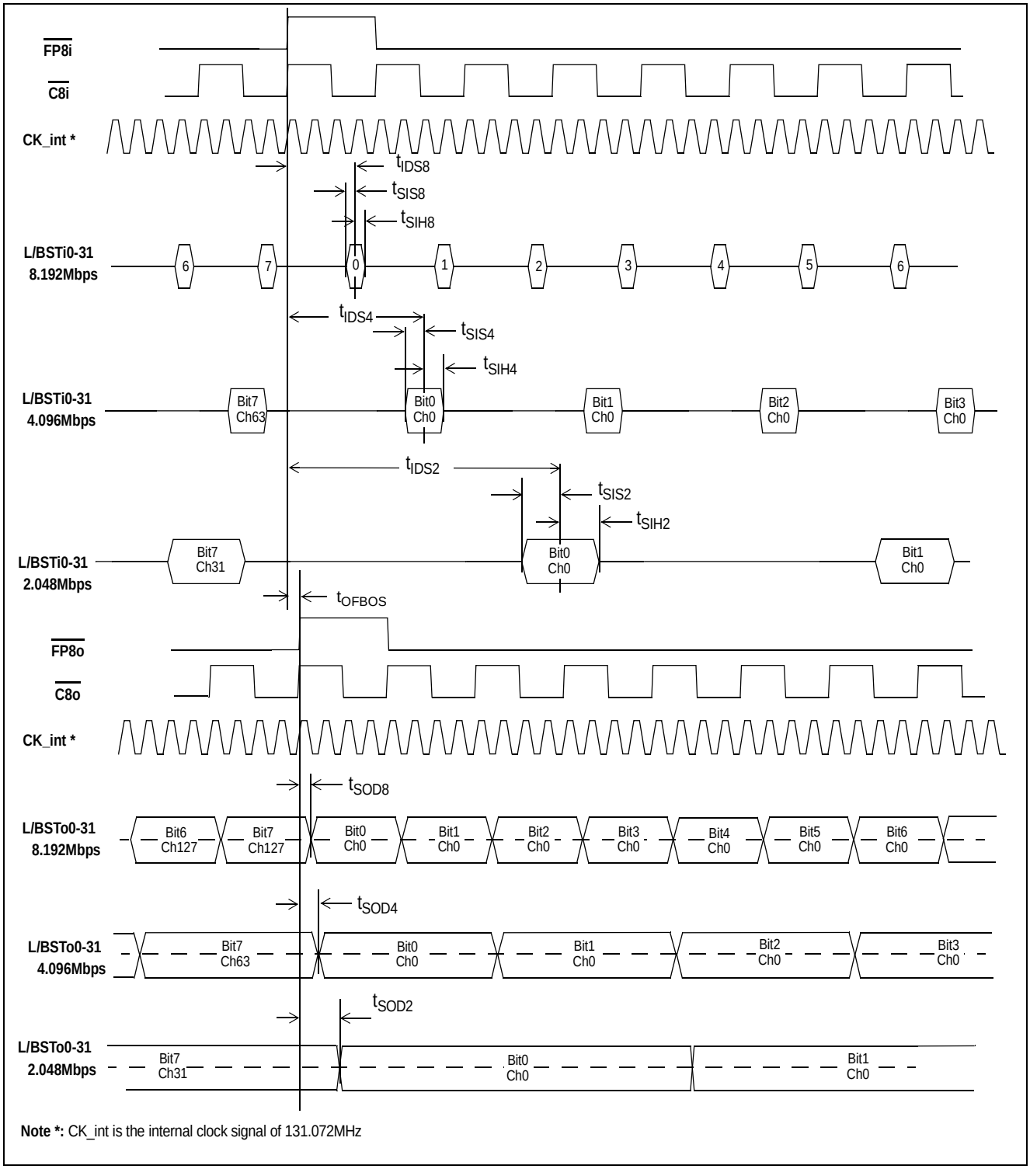
Note *: CK_int is the internal clock signal of 131.072MHz

Figure 27 - ST-BUS Local/Backplane Data Timing Diagram (8 Mbps, 4 Mbps, 2 Mbps)



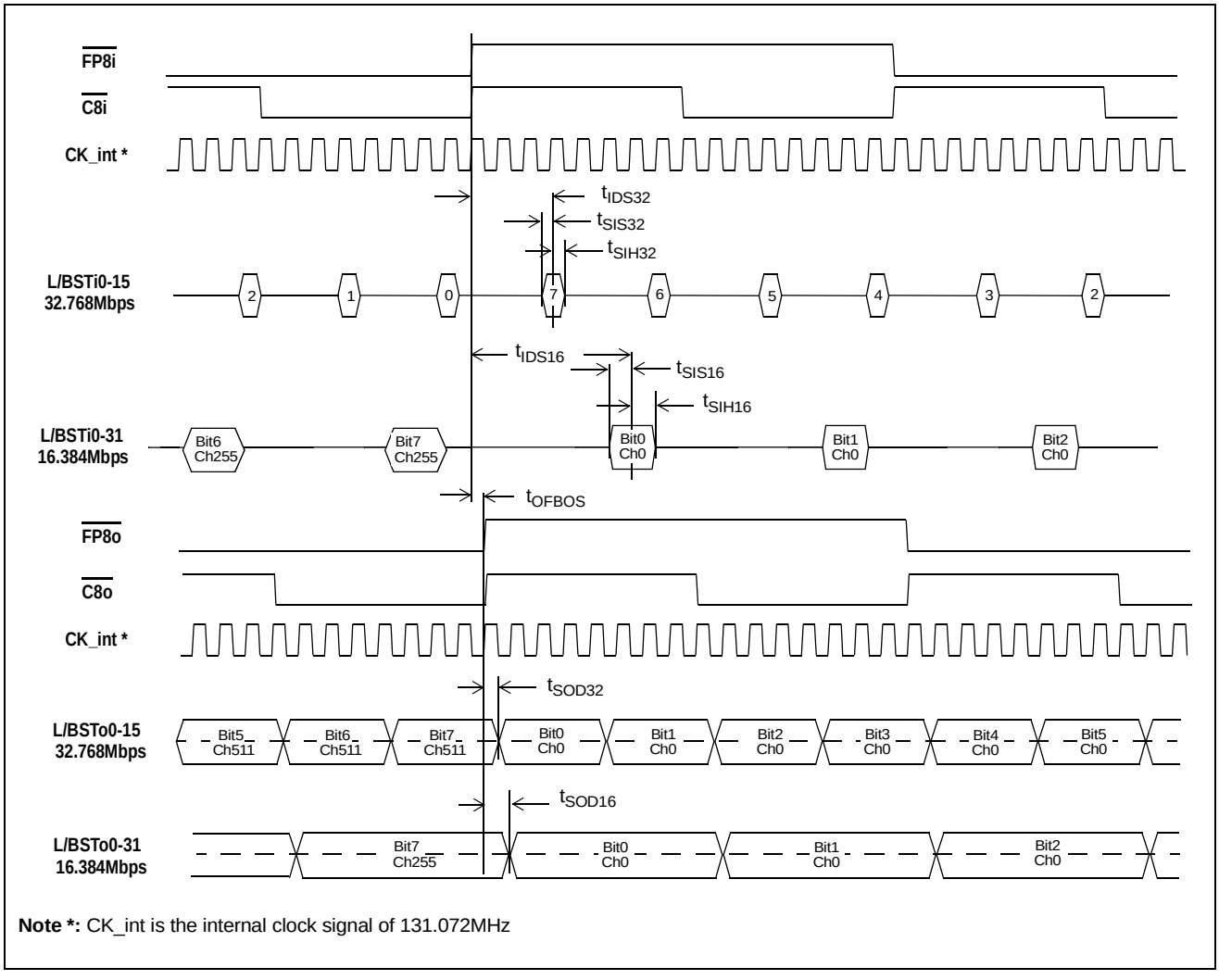
Note *: CK_int is the internal clock signal of 131.072MHz

Figure 28 - ST-BUS Local/Backplane Data Timing Diagram (32 Mbps, 16 Mbps)



Note *: CK_int is the internal clock signal of 131.072MHz

Figure 29 - GCI-Bus Local/Backplane Data Timing Diagram (8 Mbps, 4 Mbps, 2 Mbps)



Note *: CK_int is the internal clock signal of 131.072MHz

Figure 30 - GCI-Bus Local/Backplane Data Timing Diagram (32 Mbps, 16 Mbps)

Local and Backplane Output High Impedance Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	STo delay - Active to High-Z - High-Z to Active	t_{DZ} t_{ZD}		4 4	6 6	ns ns	R_L=1k, C_L=50pF, See Note 1
2	Output Driver Enable (ODE) Delay to Active Data Output Driver Enable (ODE) Delay to high impedance	t_{ODE} t_{ODZ}			14 14	ns ns	R_L=1k, C_L=50pF, See Note 1 R_L=1k, C_L=50pF, See Note 1

Note 1: High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

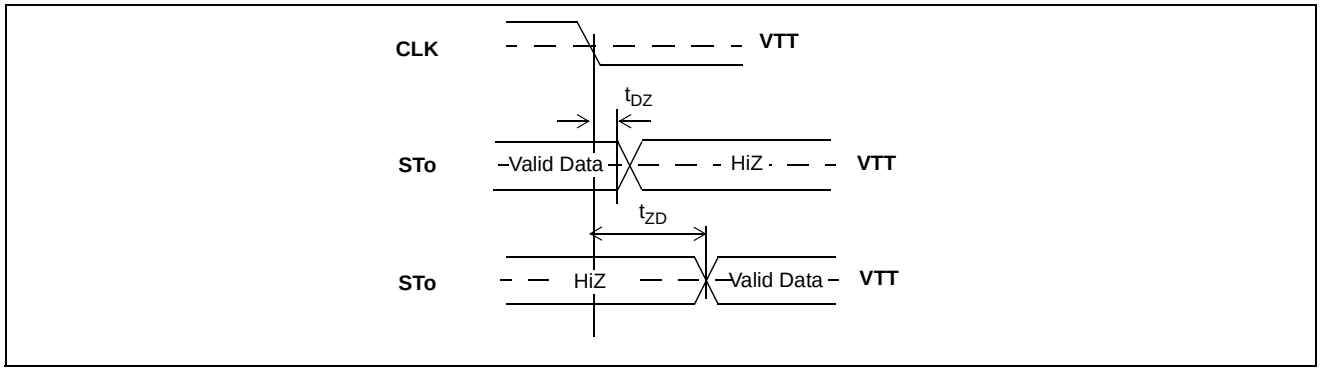


Figure 31 - Serial Output and External Control

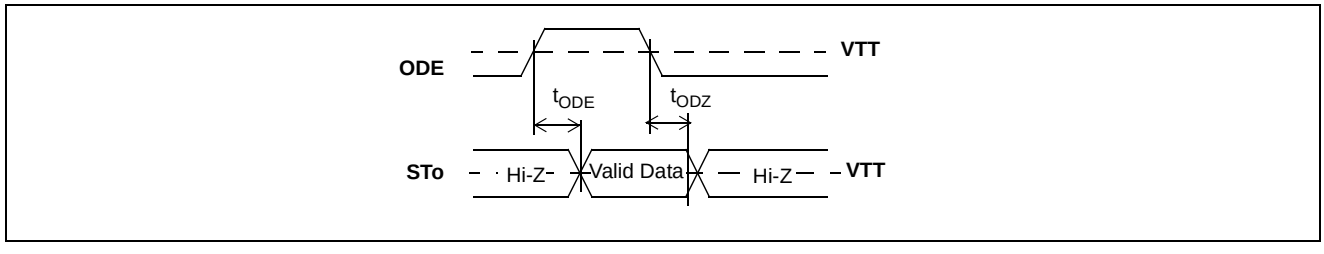


Figure 32 - Output Driver Enable (ODE)

Input Clock Jitter Tolerance

	Jitter Frequency	16.384 Mbps Data Rate Jitter Tolerance	32.768 Mbps Data Rate Jitter Tolerance	Units
1	1 kHz	1200	600	ns
2	10 kHz	1200	600	ns
3	50 kHz	150	80	ns
4	66 kHz	110	50	ns
5	83 kHz	80	35	ns
6	95 kHz	70	30	ns
7	100 kHz	25	20	ns
8	200 kHz	17	14	ns
9	300 kHz	17	14	ns
10	400 kHz	17	14	ns
11	500 kHz	17	14	ns
12	1 MHz	17	14	ns
13	2 MHz	17	14	ns
14	4 MHz	17	14	ns

Non-Multiplexed Microprocessor Port Timing

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	$\overline{CS}$ setup from $\overline{DS}$ falling	t_{CSS}	0			ns	
2	R/$\overline{W}$ setup from $\overline{DS}$ falling	t_{RWS}	9			ns	
3	Address setup from $\overline{DS}$ falling	t_{ADS}	9			ns	
4	$\overline{CS}$ hold after $\overline{DS}$ rising	t_{CSH}	0			ns	
5	R/$\overline{W}$ hold after $\overline{DS}$ rising	t_{RWH}	9			ns	
6	Address hold after $\overline{DS}$ rising	t_{ADH}	9			ns	
7	Data setup from $\overline{DTA}$ Low on Read	t_{RDS}	5 12			ns ns	Memory Read Register Read C_L=60pF
8	Data hold on read	t_{RDH}			4.5	ns	C_L=60pF, R_L=1k Note 1
9	Data setup on write	t_{WDS}	9			ns	
10	Data hold on write	t_{WDH}	9			ns	
11	Acknowledgment Delay: Reading/Writing Registers Reading/Writing Memory	t_{AKD}			 88 80	 ns ns	 C_L=60pF C_L=60pF
12	Acknowledgment Hold Time	t_{AKH}			11	ns	C_L=60pF, R_L=1k, Note 1

Note 1: High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

Note 2: There must be a minimum of 30 ns between CPU accesses, to allow the device to recognize the accesses as separate (i.e., a minimum of 30 ns must separate the de-assertion of DTA (to high) and the assertion of CS and/or DS to initiate the next access).

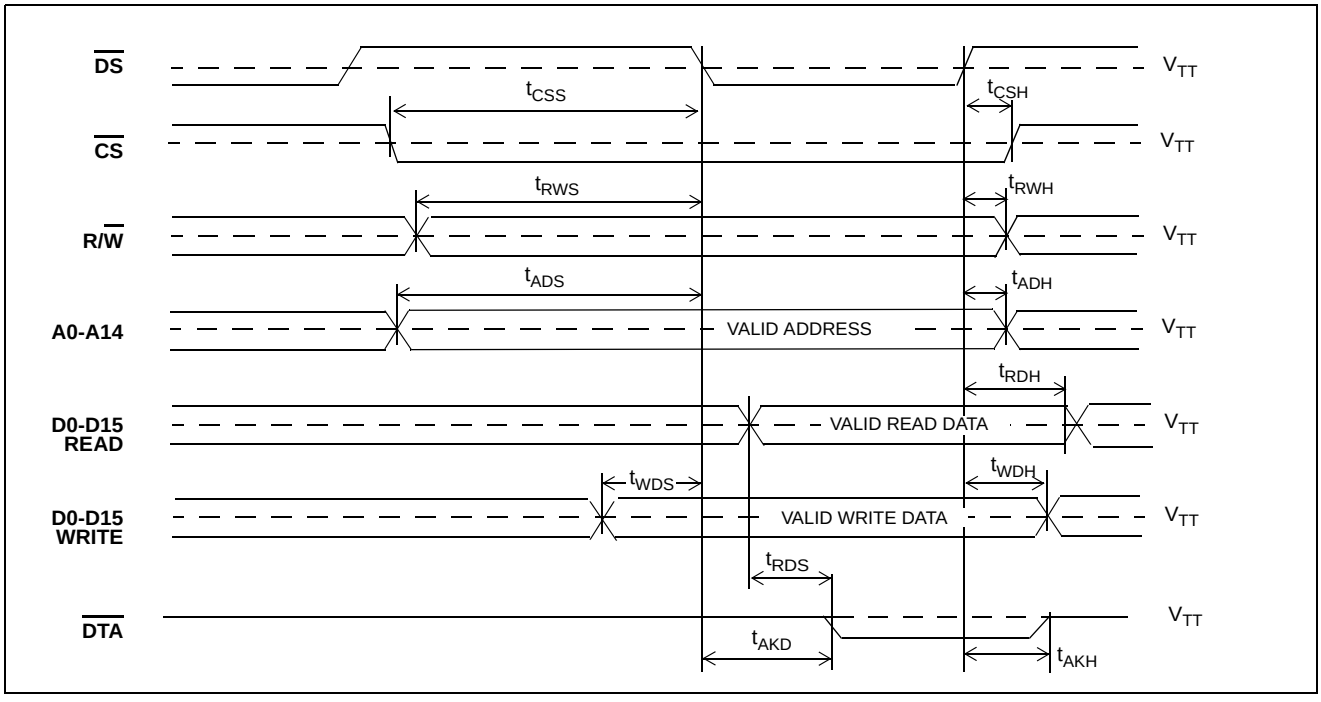


Figure 33 - Motorola Non-Multiplexed Bus Timing

AC Electrical Characteristics† - JTAG Test Port Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	TCK Clock Period	t_{TCKP}	100			ns	
2	TCK Clock Pulse Width High	t_{TCKH}	80			ns	
3	TCK Clock Pulse Width Low	t_{TCKL}	80			ns	
4	TMS Set-up Time	t_{TMSS}	10			ns	
5	TMS Hold Time	t_{TMSH}	10			ns	
6	TDi Input Set-up Time	t_{TDIS}	20			ns	
7	TDi Input Hold Time	t_{TDIH}	60			ns	
8	TDo Output Delay	t_{TDOD}			30	ns	C_L=30pF
9	$\overline{\text{TRST}}$ pulse width	t_{TRSTW}	200			ns	

†Characteristics are over recommended operating conditions unless otherwise stated.

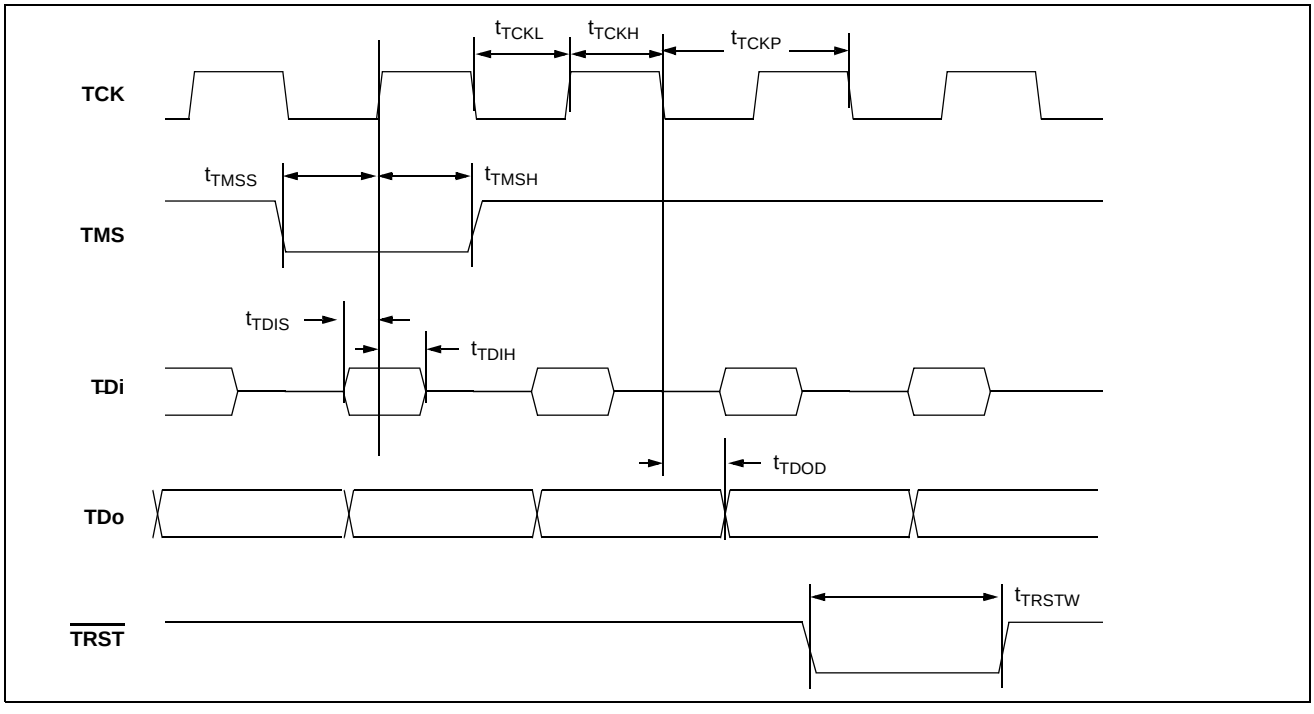
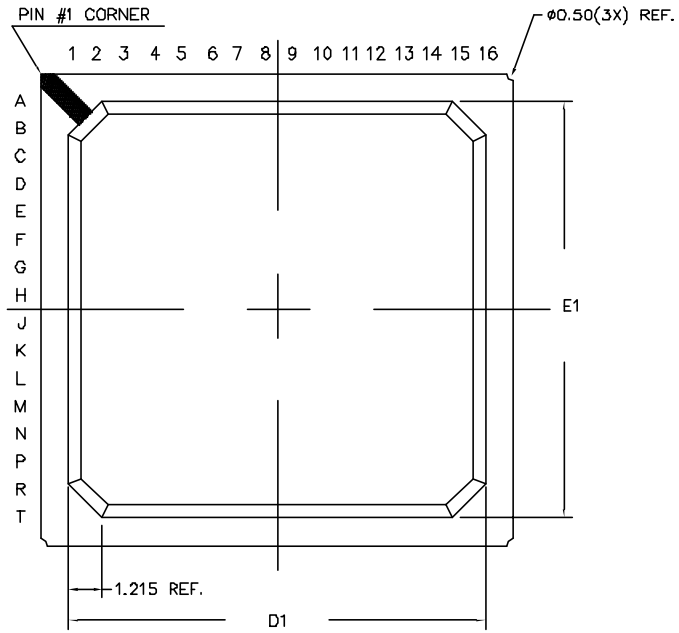
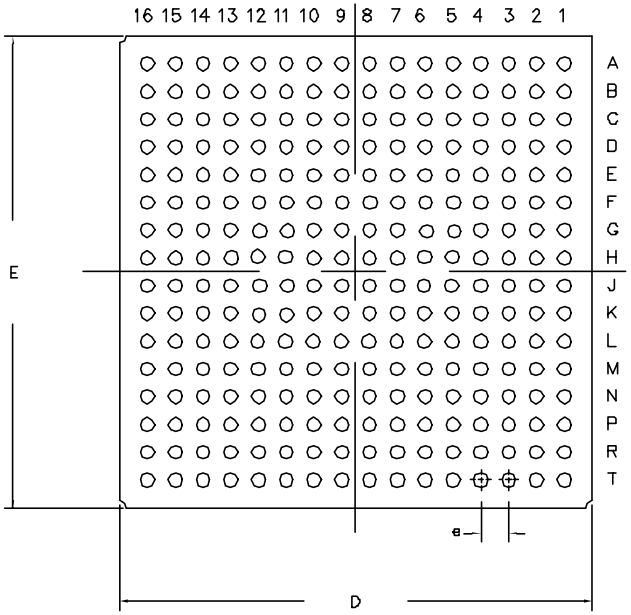


Figure 34 - JTAG Test Port Timing Diagram

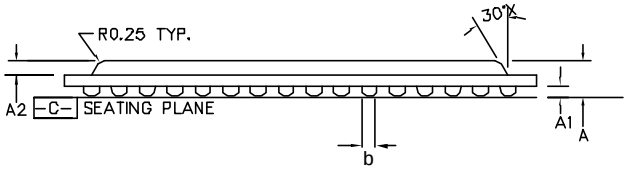
TOP VIEW



BOTTOM VIEW



DIMENSION	MIN	MAX
A	1.42	1.80
A1	0.30	0.50
A2	0.85 REF	
D	16.80	17.20
D1	14.80	15.20
E	16.80	17.20
E1	14.80	15.20
b	0.40	0.60
e	1.00	
N	256	
Conforms to JEDEC MS-034		



SIDE VIEW

NOTES: –
1. Controlling dimensions are in MM.
2. Seating plane is defined by the spherical crown of the solder balls.
3. Not to scale.
4. N is the number of solder balls
5. Substrate thickness is 0.36 MM.

ISSUE	1			
ACN	214440			
DATE	26June03			
APPRD.				

ZARLINK SEMICONDUCTOR

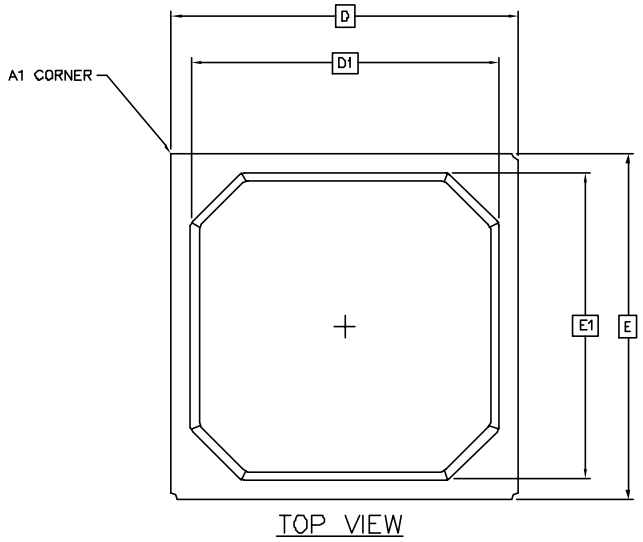
Previous package codes

BP/G

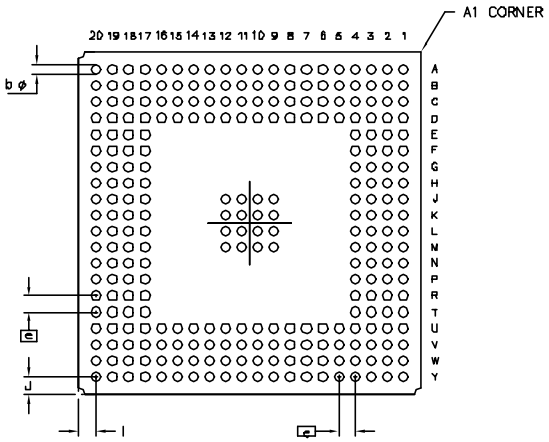
Package Code GA

Package Outline for
256ball BGA
17x17x1.61mm

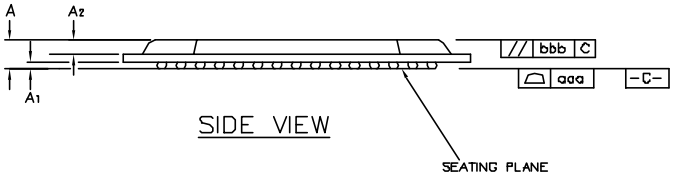
GPD00842



TOP VIEW



BOTTOM VIEW



SIDE VIEW

DIMENSION	MIN	MAX
A	1.92 (2.12)	2.32 (2.54)
A1	0.50	0.70
A2	1.12	1.22
D	26.80	27.20
D1	---	24.70
E	26.80	27.20
E1	---	24.70
I	1.44 REF.	
J	1.44 REF.	
b	0.60	0.90
e	1.27 BSC	
N	272	
2 LAYERS (4 LAYERS)		

Conforms to JEDEC MS-034 BAL-2 Iss. A

NOTE:
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER
3. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. ALL DIMENSIONS ARE IN MILLIMETERS.

ISSUE	1	2	3	
ACN	207257	209824	213917	
DATE	16AUG99	3NOV00	13Jan03	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes:
BP / G

Package Code GA

Package Outline for 272 Ball PBGA (27 x 27mm)

GPD00588

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www.zarlink.com