

MYC-C7Z010/20-V2 CPU Module

- Xilinx XC7Z010/20 Dual-core ARM Cortex-A9 Processor with Xilinx 7-series FPGA logic
- 1GB DDR3 SDRAM (2 x 512MB, 32-bit), 4GB eMMC, 32MB QSPI Flash
- On-board Gigabit Ethernet PHY
- Two 0.8mm pitch 140-pin Board-to-Board Expansion Connectors
- Ready-to-Run Linux 5.4.0



Figure 1-1 MYC-C7Z010/20-V2 Top-view



Figure 1-2 MYC-C7Z010/20-V2 CPU Bottom-view

The [MYC-C7Z010/20-V2 CPU Module](#) is a Linux-ready ZYNQ-based SOM (System on Module) available for either Xilinx XC7Z010 or XC7Z020 device. It integrates Xilinx's Dual Cortex-A9 + FPGA All Programmable SoC device, 1GB DDR3 SDRAM, 4GB eMMC, 32MB quad SPI Flash, a Gigabit Ethernet PHY, a USB PHY and external watchdog. Two 0.8mm pitch 140-pin board-to-board connectors provide a large number of I/O signals for ARM peripherals and FPGA I/Os to enable your base board extension. It is ideal for your next embedded design, thus helping you reduce development effort and speed up your time to market.

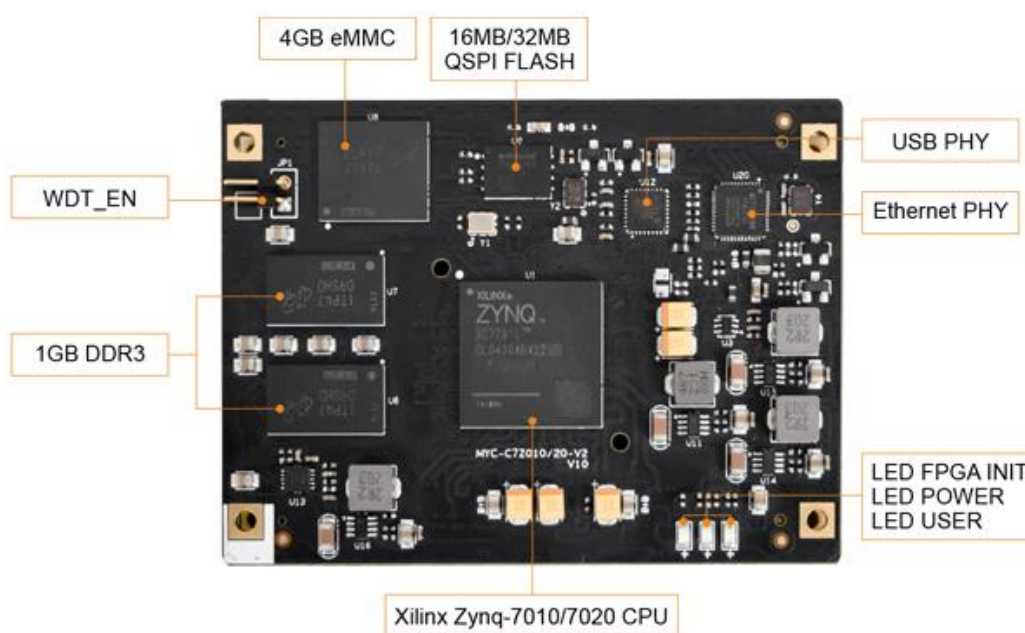


Figure 1-3 MYC-C7Z010/20-V2 CPU Module

The MYC-C7Z010/20-V2 CPU Module is the core board of MYD-C7Z010/20-V2 development board which is an excellent platform for evaluation and prototype based on MYIR's MYC-C7Z010/20-V2 CPU module. It takes full features of the Zynq-7010 and 7020 SoC and has extended rich peripherals to the base board including four USB Host ports, RS232 serial port, Gigabit Ethernet, CAN, LCD and HDMI. It has one XADC header to allow you take advantage of Xilinx XADC; it has three PMoD headers to meet your I/O needs with PMoDs (only for 7020); it also has a low-pin count FMC connector to allow various FMC cards for custom I/O options. Typical applications are Industrial Automation, Test & measurement, Medical Equipment, Intelligent Video Surveillance, etc.

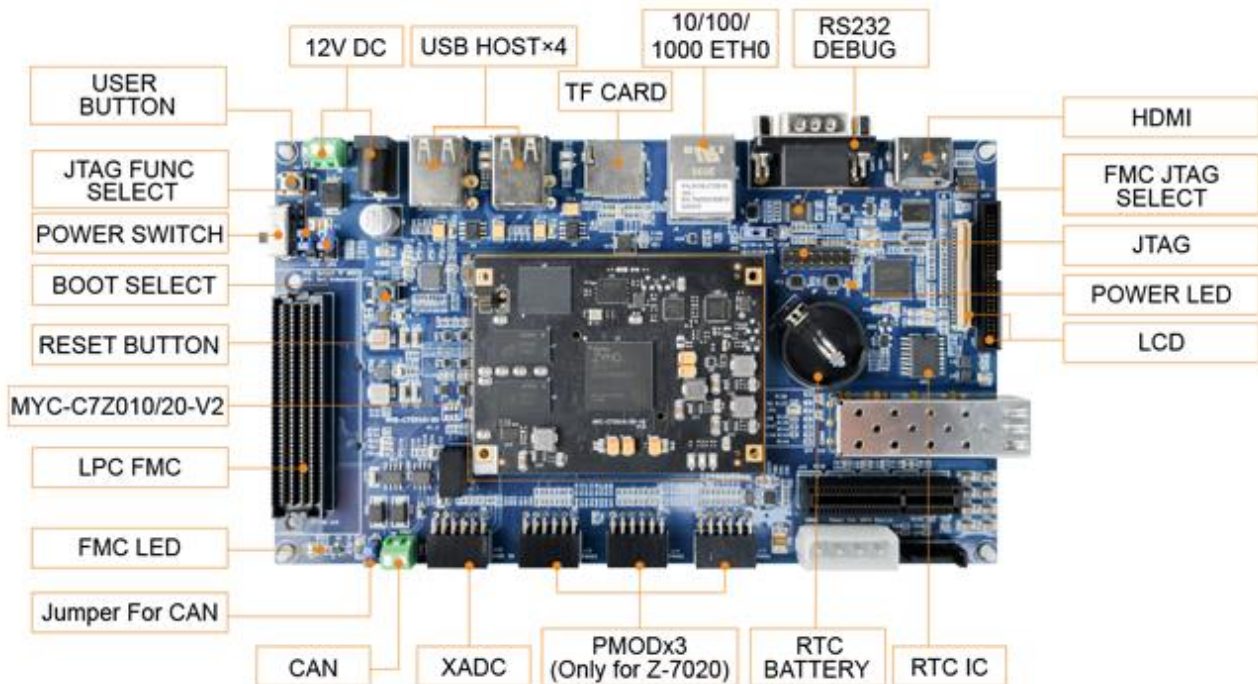


Figure 1-4 MYD-C7Z010/20 Development Board

Hardware Specification

The Zynq™-7000 family of devices combines the software programmability of a Processor with the hardware programmability of an FPGA, resulting in unrivaled levels of system performance, flexibility, scalability while providing system benefits in terms of power reduction, lower cost with fast time to market. Unlike traditional SoC processing solutions, the flexible programmable logic of the Zynq-7000 devices enables optimization and differentiation, allowing designers to add peripherals and accelerators to adapt to a broad base of applications.

The Zynq-7000 AP SoC leverages the 28nm scalable optimized programmable logic used in Xilinx's 7 series FPGAs. Each device is designed to meet unique requirements across many use cases and applications. The Z-7010, Z-7015, and Z-7020 leverage the Artix®-7 FPGA programmable logic and offer lower power and lower cost for high-volume applications. The Z-7030, Z-7035, Z-7045, and Z-7100 are based on the Kintex®-7 FPGA programmable logic for higher-end applications that require higher performance and high I/O throughput.

	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™						
Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor						
L1 Cache	32 KB Instruction, 32 KB Data per processor						
L2 Cache	512 KB						
On-Chip Memory	256 KB						
Memory Interfaces	DDR3, DDR3L, DDR2, LPDDR2, 2x Quad-SPI, NAND, NOR						
Peripherals	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO						
Logic Cells	28K Logic Cells	74K Logic Cells	85K Logic Cells	125K Logic Cells	275K Logic Cells	350K Logic Cells	444K Logic Cells
BlockRAM (Mb)	240 KB	380 KB	560 KB	1,060 KB	2,000 KB	2,180 KB	3,020 KB
DSP Slices	80	160	220	400	900	900	2,020
Transceiver Count		4 (6.25 Gb/s)		up to 4 (12.5 Gb/s)	up to 16 (12.5 Gb/s)	up to 16 (12.5 Gb/s)	up to 16 (10.3125 Gb/s)

Table 1-1 ZYNQ-7000 Devices

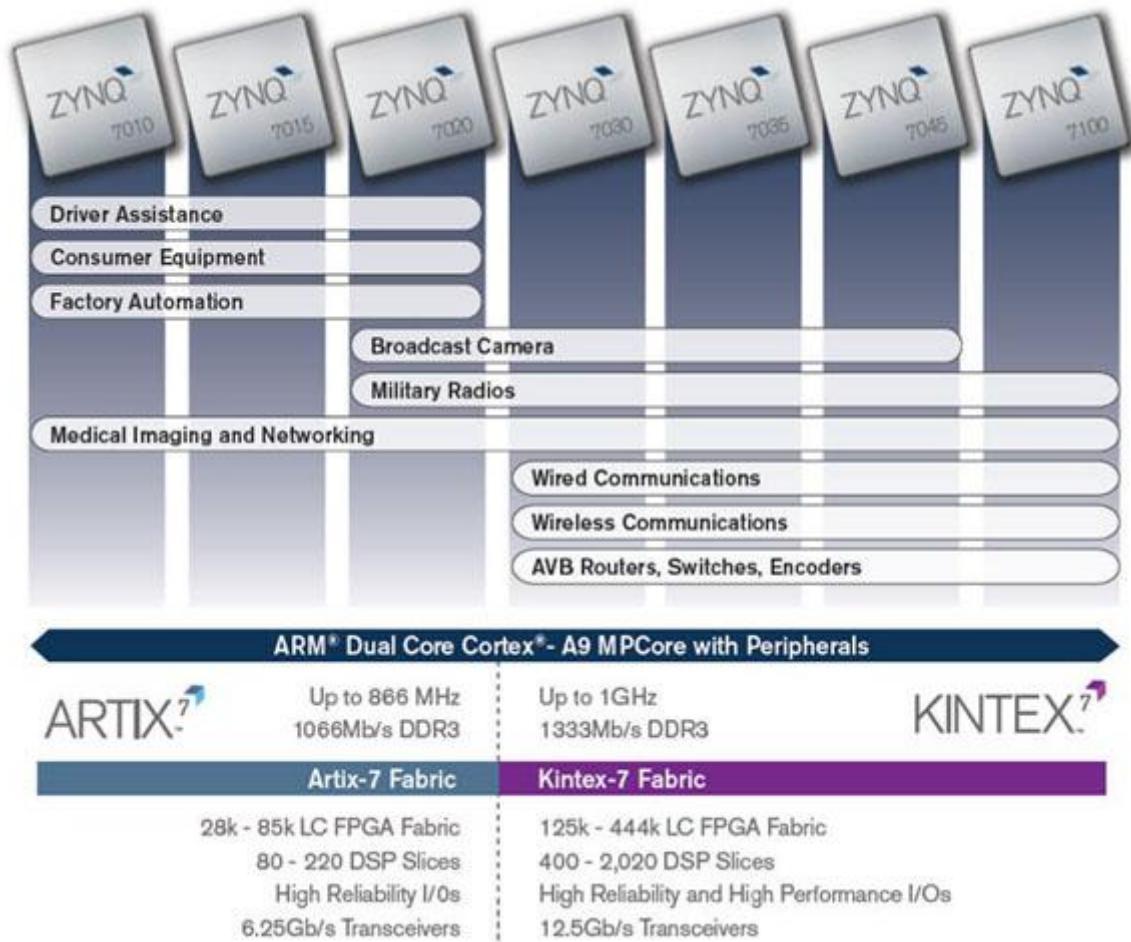


Figure 1-5 Zynq-7000 Devices

Mechanical Parameters

- ✓ Dimensions: 75mm x 55mm (10-layer PCB design)
- ✓ Power supply: 5V/0.5A
- ✓ Working temp.: 0~70 Celsius (commercial grade) or -40~85 Celsius (industrial grade)

SoC

- ✓ Xilinx XC7Z010-1CLG400C (Zynq-7010) or XC7Z020-1CLG400C (Zynq-7020)
 - 667MHz ARM® dual-core Cortex™-A9 MPCore processor (up to 866MHz)
 - Integrated Artix-7 class FPGA subsystem
 - with 28K logic cells, 17,600 LUTs, 80 DSP slices (for XC7Z010)
 - with 85K logic cells, 53,200 LUTs, 220 DSP slices (for XC7Z020)
 - NEON™ & Single / Double Precision Floating Point for each processor
 - Supports a Variety of Static and Dynamic Memory Interfaces

Memory

- ✓ 1GB DDR3 SDRAM (512MB*2)
- ✓ 4GB eMMC
- ✓ 32MB QSPI Flash (16MB is optional)

Peripherals and Signals Routed to Pins

- ✓ 10/100/1000M Ethernet PHY (YT8531SH)
- ✓ External watchdog
- ✓ Three LEDs
 - One blue LED for power indicator
 - One red LED for FPGA program done indicator
 - One green user LED
- ✓ Two 0.8mm pitch 140-pin board-to-board expansion connectors bring out below signals:
 - One Gigabit Ethernet
 - One USB OTG 2.0
 - Two Serial ports
 - Two I2C
 - Two CAN BUS
- * Serial ports, I2C and CAN signals will be reused in PS part, or implemented through PL pins*
 - Two SPI (can be implemented through PL pins)
 - ADC (one independent differential ADC, 16-channel ADC brought out through PL pins)
 - One SDIO

Function Block Diagram

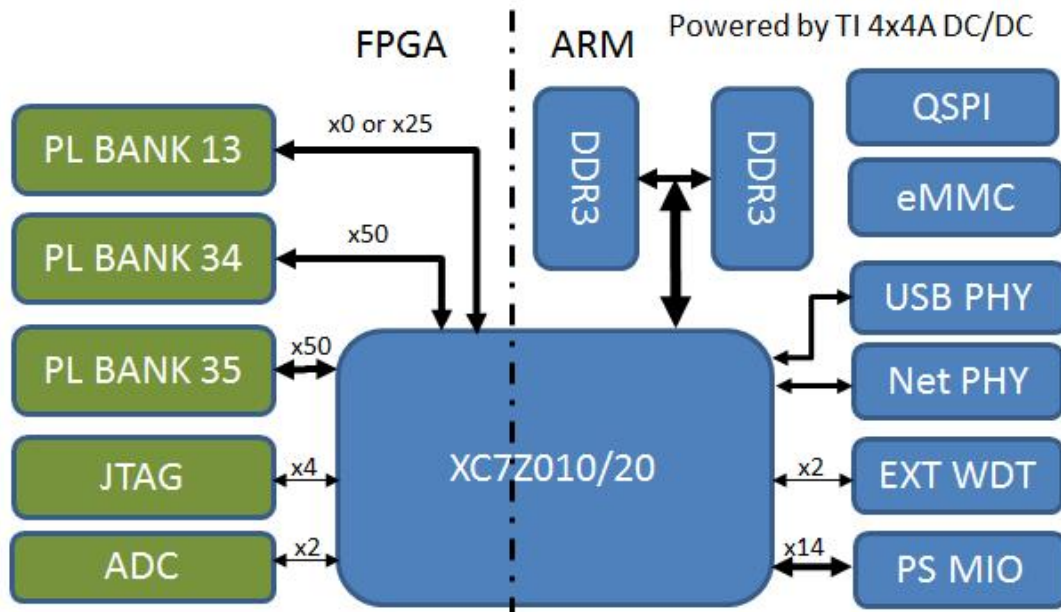


Figure 1-6 MYC-C7Z010/20-V2 Function Block Diagram

Dimension Chart

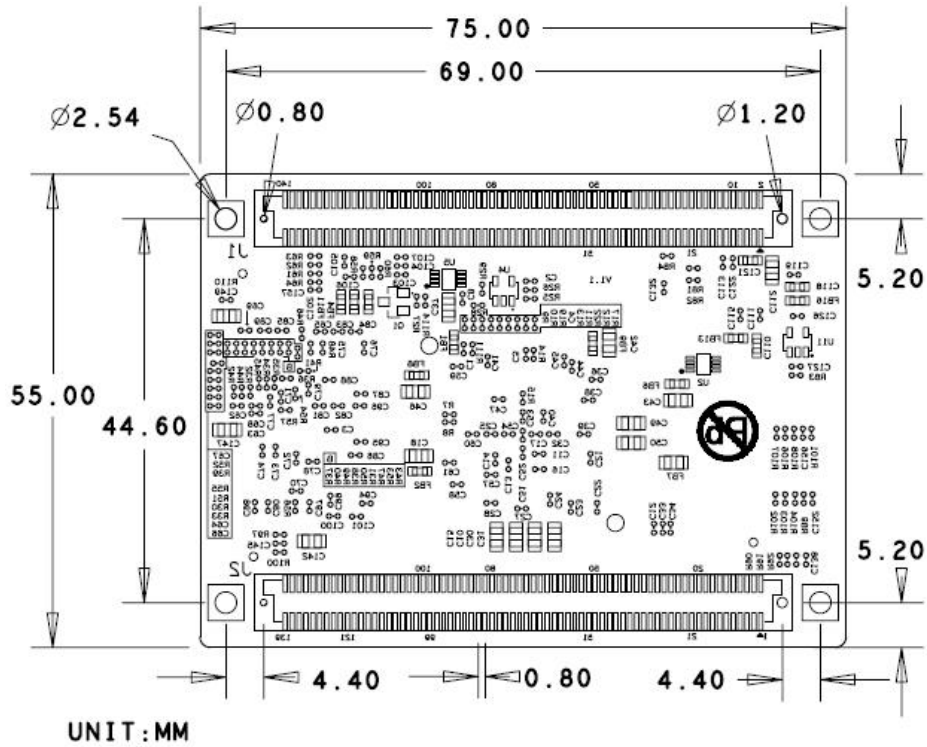


Figure 1-7 Dimensions of MYC-C7Z010/20-V2

Expansion Connectors

The MYC-C7Z010/20-V2 CPU Module is using two 0.8mm pitch 140-pin board-to-board female connectors for extension. Please refer to the file “MYC-C7Z010/020 Pin description Table” to know the signals routed to the connectors.

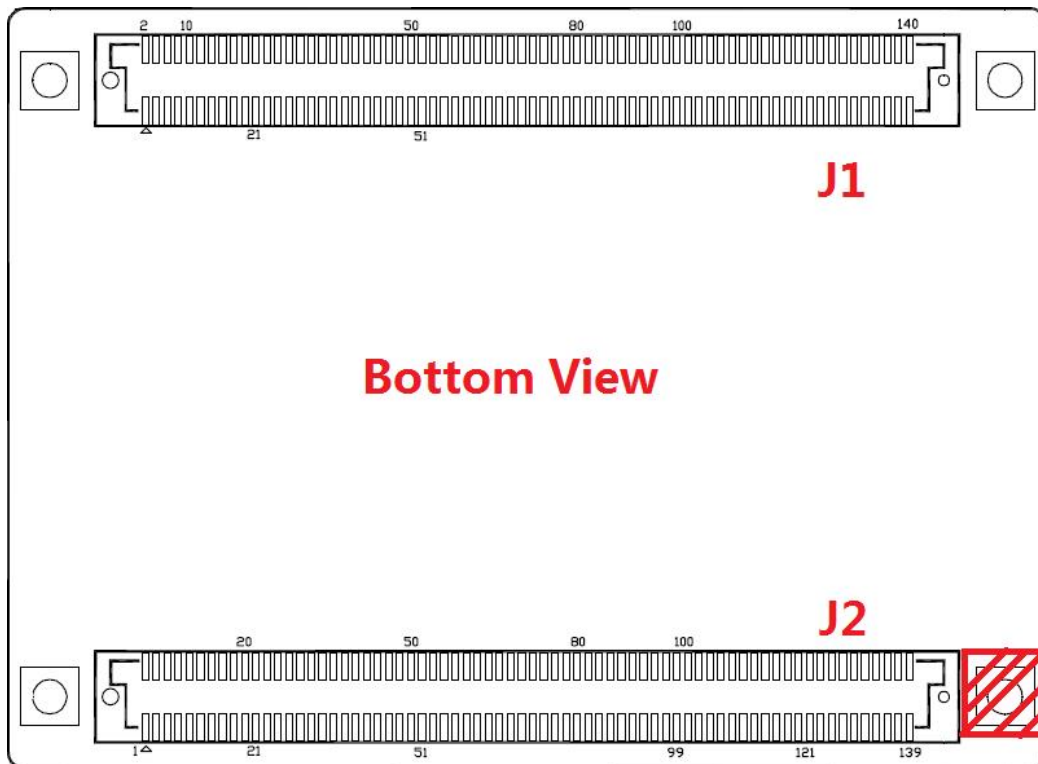


Figure 1-8 Expansion Connectors of MYC-C7Z010/20-V2

Software Features

The MYC-C7Z010/20-V2 CPU Module is capable of running Linux 4.14.0. MYIR provides software package in product disk along with the goods delivery. The software package features as below:

Item	Features	Description	Remark
Cross compiler	gcc 9.2.0	arm-xilinx-linux-gnueabi-gcc (GCC) 9.2.0	
Boot program	BOOT.BIN	First boot program including FSBL, bitstream	Source code provided
	u-boot	Secondary boot program	Source code provided
Linux Kernel	Linux 5.4.0	Customized kernel for MYD-C7Z010/20-V2	Source code provided
Drivers	USB Host	USB Host driver	Source code provided
	Ethernet	Gigabit Ethernet driver	Source code provided
	MMC/SD/TF	MMC/SD/TF card driver	Source code provided
	CAN	CAN driver	Source code provided
	LCD Controller	XYLON LCD driver	Source code provided
	HDMI	HDMI (SII902X chip) driver	Source code provided
	Button	Button driver	Source code provided
	UART	UART driver	Source code provided
	LED	LED driver	Source code provided
	GPIO	GPIO driver	Source code provided
	QSPI	QSPI Flash S25FL256S driver	Source code provided
	RTC	DS3231 RTC driver	Source code provided
	Resistive Touch	TSC2007 resistive touch screen driver	Source code provided
	Capacitive Touch	FT5X0X capacitive touch screen driver	Source code provided
ADC	ADC driver	Source code provided	
File System	Ramdisk	Ramdisk system image	
	Rootfs.tar	Tar file	

Table 1-2 Linux Software Package Features

Order Information

Item	Part No.	Packing List
MYC-C7Z020-V2 CPU Module	MYC-C7Z010-V2-4E1D-667-C	➤ One MYC-C7Z010-V2 CPU Module (for Zynq-7010)
	MYC-C7Z010-V2-4E1D-667-I	
	MYC-C7Z020-V2-4E1D-766-C	➤ One MYC-C7Z020-V2 CPU Module (for Zynq-7020)
	MYC-C7Z020-V2-4E1D-766-I	
MYD-C7Z020-V2 Development Board	MYD-C7Z010-V2-4E1D-667-C	- One MYD-C7Z010-V2 or MYD-C7Z020-V2 board (includes one CPU module MYC-C7Z010/20-V2 mounted on the base board)
	MYD-C7Z010-V2-4E1D-667-I	
	MYD-C7Z020-V2-4E1D-766-C	- One 1.5m cross Ethernet cable - One DB9 UART to USB cable - One HDMI cable - One 12V/1.25A Power adapter - One 16GB TF Card
	MYD-C7Z020-V2-4E1D-766-I	
Note: Customer may have used V1 version (MYC-C7Z010/20) before, V2 version is fully compatible with V1 version but using different Ethernet PHY chip.		


MYIR Tech Limited

Room 04, 6th Floor, Building No.2, Fada Road, Yunli Smart Park,
Bantian, Longgang District, Shenzhen, Guangdong, China 518129

E-mail: sales@myirtech.com

Phone: +86-755-22984836

Fax: +86-755-25532724

Website: <http://www.myirtech.com>