

**NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT
HC55185**

Extended Reach Ringing SLIC Family

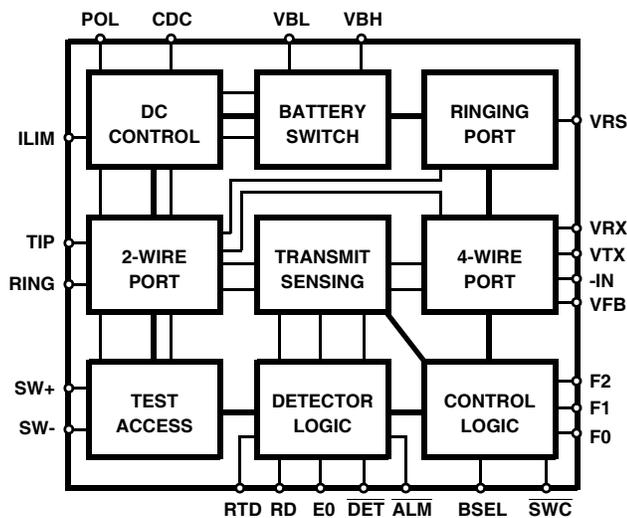
The RSLIC18™ family of ringing subscriber line interface circuits (RSLIC) supports analog Plain Old Telephone Service (POTS) in short and medium loop length, wireless and wireline applications. Ideally suited for remote subscriber units, this family of products offers flexibility to designers with high ringing voltage and low power consumption system requirements.

The HC55183 and HC55184 family operates up to 75V, and the HC55185 family operates to 100V, which translates directly to the amount of ringing voltage supplied to the end subscriber. With 100V operating voltage, subscriber loop lengths can be extended up to 500Ω (i.e., 5,000 feet) and beyond.

Other key features across the product family include: low power consumption, ringing using sinusoidal or trapezoidal waveforms, robust auto-detection mechanisms for when subscribers go on or off hook, and minimal external discrete application components. Integrated test access features are also offered on selected products to support loopback testing as well as line measurement tests.

There are 2 product offerings in the RSLIC18 family: HC55183 and HC55184. The architecture for this family is based on a voltage feed amplifier design using low fixed loop gains to achieve high analog performance with low susceptibility to system induced noise.

Block Diagram



Features

- Battery Operation to 75V
- Low Standby Power Consumption of 50mW
- Peak Ringing Amplitude 95V, 5 REN
- Sinusoidal or Trapezoidal Ringing Capability
- Integrated CODEC Ringing Interface
- Integrated MTU DC Characteristics
- Low External Component Count
- Pulse Metering and On Hook Transmission
- Tip Open Ground Start Operation
- Thermal Shutdown with Alarm Indicator
- 28 Lead Surface Mount Packaging
- Dielectric Isolated (DI) High Voltage Design
- HC55183
 - Integrated Battery Switch
 - 45dB Longitudinal Balance
- HC55184
 - Integrated Battery Switch
 - Silent Polarity Reversal
 - 45dB Longitudinal Balance
- Pb-Free (RoHS Compliant)

Applications

- Wireless Local Loop (WLL)
- Digital Added Main Line (DAML)/Pairgain
- Integrated Services Digital Network (ISDN)
- Small Office Home Office (SOHO) PBX
- Cable/Computer Telephony

Related Literature

- AN9824, Spice Model Tutorial of the RSLIC18 AC Loop

Ordering Information (PLCC Package Only)

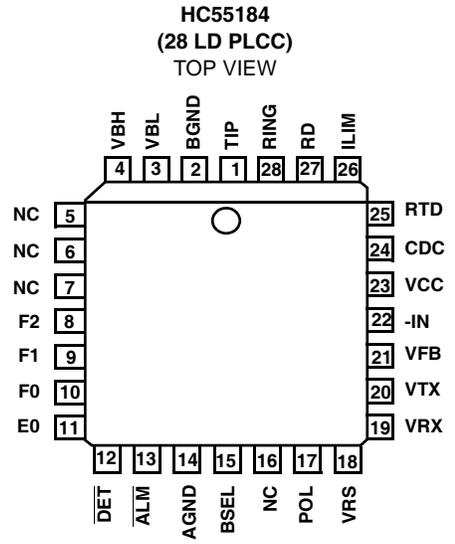
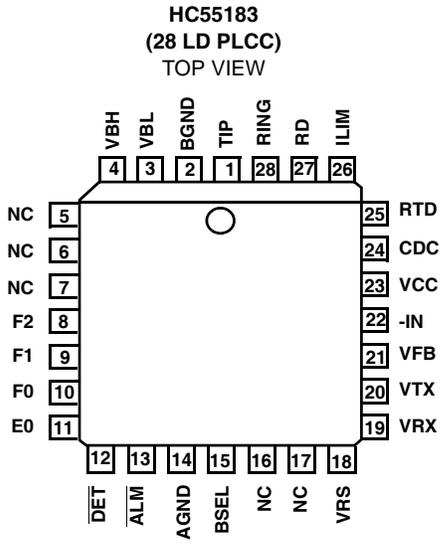
PART NUMBER	100V	85V	BAT SW	POL REV	FULL TEST	LOOP BACK ONLY	LB = 53dB	LB = 58dB	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HC55183ECMZ (Note)		75V	•				45dB		0 to +70	28 Ld PLCC (Pb-free)	N28.45
HC55183ECMZ96 (Note)		75V	•				45dB		0 to +70	28 Ld PLCC (Pb-free)	N28.45
HC55184ECMZ (Note)		75V	•	•			45dB		0 to +70	28 Ld PLCC (Pb-free)	N28.45
HC55184ECMZR4749 (Note)		75V	•	•			45dB		0 to +70	28 Ld PLCC (Pb-free)	N28.45
HC55184ECMZ96R4749 (Note)		75V	•	•			45dB		0 to +70	28 Ld PLCC (Pb-free)	N28.45

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Device Operating Modes

OPERATING MODE	F2	F1	F0	E0 = 1	E0 = 0	DESCRIPTION	HC55183	HC55184
Low Power Standby	0	0	0	SHD	GKD	MTU compliant standby mode with active loop detector.	•	•
Forward Active	0	0	1	SHD	GKD	Forward battery loop feed.	•	•
Unused	0	1	0	n/a	n/a	This is a reserved internal test mode.		
Reverse Active	0	1	1	SHD	GKD	Reverse battery loop feed.		•
Ringling	1	0	0	RTD	RTD	Balanced ringling mode supporting both sinusoidal, trapezoidal and ringling waveforms with DC offset.	•	•
Forward Loop Back	1	0	1	SHD	GKD	Internal device test mode.		
Tip Open	1	1	0	SHD	GKD	Tip amplifier disabled and ring amplifier enabled. Intended for PBX type applications.		
Power Denial	1	1	1	n/a	n/a	Device shutdown.	•	•

Pinouts



HC55183, HC55184

Absolute Maximum Ratings $T_A = 25^\circ\text{C}$

Maximum Supply Voltages	
V_{CC}	-0.5V to +7V
$V_{CC} - V_{BAT}$	85V
Uncommitted Switch Voltage	-110V
Maximum Tip/Ring Negative Voltage Pulse (Note 17)	-115V
Maximum Tip/Ring Positive Voltage Pulse (Note 17)8V
ESD (Human Body Model)	500V

Operating Conditions

Temperature Range	
Commercial (C Suffix)	0°C to $+70^\circ\text{C}$
Positive Power Supply (V_{CC})	$+5\text{V} \pm 5\%$
Negative Power Supply (V_{BH} , V_{BL})	-24V to -75V
Uncommitted Switch (loop back or relay driver)	$+5\text{V}$ to -100V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^\circ\text{C}/\text{W}$)
PLCC Package	55
Maximum Junction Temperature Plastic	$+150^\circ\text{C}$
Maximum Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Pb-Free Reflow Profile see link below	
http://www.intersil.com/pbfree/Pb-FreeReflow.asp	

Die Characteristics

Substrate Potential	V_{BAT}
Process	Bipolar-DI

Electrical Specifications Unless Otherwise Specified, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{BL} = -24\text{V}$, $V_{BH} = -85\text{V}$ or -75V , $V_{CC} = +5\text{V}$, $AGND = BGND = 0\text{V}$, loop current limit = 25mA. All AC Parameters are specified at 600 Ω 2-wire terminating impedance over the frequency band of 300Hz to 3.4kHz. Protection resistors = 0 Ω . These parameters apply generically to each product offering.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RINGING PARAMETERS (Note 2)					
VRS Input Impedance (Note 3)		480	-	-	k Ω
Differential Ringing Gain	VRS to 2-Wire, $R_{LOAD} = \infty$ (Note 4)	78	80	82	V/V
4-Wire to 2-Wire Ringing Off Isolation	Active mode, referenced to VRS input.	-	60	-	dB
2-Wire to 4-Wire Transmit Isolation	Ringing mode referenced to the differential ringing amplitude.	-	60	-	dB
AC TRANSMISSION PARAMETERS (Notes 5, 6)					
Receive Input Impedance (Note 3)		160	-	-	k Ω
Transmit Output Impedance (Note 3)		-	-	1	Ω
4-Wire Port Overload Level	THD = 1%	3.1	3.5	-	V_{PK}
2-Wire Port Overload Level	THD = 1%	3.1	3.5	-	V_{PK}
2-Wire Return Loss	f = 300Hz	-	26	-	dB
	f = 1kHz	-	32	-	dB
	f = 2.3kHz	-	21	-	dB
	f = 3.4kHz	-	17	-	dB
Longitudinal Current Capability (Per Wire) (Note 3)	Test for False Detect	20	-	-	mA _{RMS}
	Test for False Detect, Low Power Standby	10	-	-	mA _{RMS}
4-Wire to 2-Wire Insertion Loss		-0.20	0.0	+0.30	dB
2-Wire to 4-Wire Insertion Loss		-6.22	-6.02	-5.82	dB
4-Wire to 4-Wire Insertion Loss		-6.32	-6.02	-5.82	dB
Idle Channel Noise 2-Wire	C-Message	-	16	19	dBrnC
	Psophometric	-	-73.5	-71	dBmp
Idle Channel Noise 4-Wire	C-Message	-	10	13	dBrnC
	Psophometric	-	-79.5	-77	dBmp

HC55183, HC55184

Electrical Specifications Unless Otherwise Specified, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{BL} = -24\text{V}$, $V_{BH} = -85\text{V}$ or -75V , $V_{CC} = +5\text{V}$, $AGND = BGND = 0\text{V}$, loop current limit = 25mA. All AC Parameters are specified at 600Ω 2-wire terminating impedance over the frequency band of 300Hz to 3.4kHz. Protection resistors = 0Ω . These parameters apply generically to each product offering. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC PARAMETERS (Note 6)					
Loop Current Limit Programming Range (Note 5)	Max Low Battery = -52V	15	-	45	mA
Loop Current During Low Power Standby	Forward polarity only.	18	-	26	mA
LOOP DETECTORS AND SUPERVISORY FUNCTIONS					
Switch Hook Programming Range		5	-	15	mA
Switch Hook Programming Accuracy	Assumes 1% external programming resistor	-	± 2	± 10	%
Dial Pulse Distortion		-	1.0	-	%
Ring Trip Comparator Threshold		2.4	2.7	3.0	V
Ring Trip Programming Current Accuracy		-	-	± 10	%
Ground Key Threshold		-	12	-	mA
Thermal Alarm Output	IC junction temperature	-	175	-	$^\circ\text{C}$
LOGIC INPUTS (F0, F1, F2, E0, SWC, BSEL)					
Input Low Voltage		-	-	0.8	V
Input High Voltage		2.0	-	-	V
Input Low Current	$V_{IL} = 0.4\text{V}$	-20	-	-	μA
Input High Current	$V_{IH} = 2.4\text{V}$	-	-	5	μA
LOGIC OUTPUTS ($\overline{\text{DET}}$, $\overline{\text{ALM}}$)					
Output Low Voltage	$I_{OL} = 5\text{mA}$	-	-	0.4	V
Output High Voltage	$I_{OH} = 100\mu\text{A}$	2.4	-	-	V
POWER SUPPLY REJECTION RATIO					
V_{CC} to 2-Wire	$f = 300\text{Hz}$	-	40	-	dB
	$f = 1\text{kHz}$	-	35	-	dB
	$f = 3.4\text{kHz}$	-	28	-	dB
V_{CC} to 4-Wire	$f = 300\text{Hz}$	-	45	-	dB
	$f = 1\text{kHz}$	-	43	-	dB
	$f = 3.4\text{kHz}$	-	33	-	dB
V_{BL} to 2-Wire	$300\text{Hz} \leq f \leq 3.4\text{kHz}$	-	30	-	dB
V_{BL} to 4-Wire	$300\text{Hz} \leq f \leq 3.4\text{kHz}$	-	35	-	dB
V_{BH} to 2-Wire	$300\text{Hz} \leq f \leq 3.4\text{kHz}$	-	33	-	dB
V_{BH} to 4-Wire	$300\text{Hz} \leq f \leq 1\text{kHz}$	-	40	-	dB
	$1\text{kHz} < f \leq 3.4\text{kHz}$	-	45	-	dB

NOTES:

2. These parameters are specified at high battery operation. BSEL = 1.
3. These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
4. Differential Ringing Gain is measured with $V_{RS} = 0.663 V_{RMS}$ for -85V devices and $V_{RS} = 0.575 V_{RMS}$ for -75V devices.
5. These parameters are specified at low battery operation. The external supply is set to BSEL = 0.
6. Forward Active and Reverse Active performance is guaranteed for the HC55184 device only. The HC55183 is specified for Forward Active operation only.

HC55183, HC55184

Electrical Specifications Unless Otherwise Specified, $T_A = 0^\circ\text{C}$ to 70°C , $V_{BL} = -24\text{V}$, $V_{CC} = +5\text{V}$, $AGND = BGND = 0\text{V}$, loop current limit = 25mA. All AC Parameters are specified at 600Ω 2-wire terminating impedance over the frequency band of 300Hz to 3.4kHz. Protection resistors = 0Ω.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RINGING PARAMETERS (Note 2)					
Ringing Voltage Open Circuit (Note 7)	THD \leq 0.5% $V_{BH} = -75\text{V}$	70	-	-	V_{PEAK}
	(Note 8)	-	-	-	V_{PEAK}
Ringing Voltage Load = 1.3K (Notes 7, 9)	THD \leq 3.0% $V_{BH} = -75\text{V}$	70	-	-	V_{PEAK}
	(Note 8)	-	-	-	V_{PEAK}
Tip Centering Voltage	$V_{BH} = -75\text{V}$, $R_L = \infty$	-	-	± 3	V
	(Note 8)	-	-	-	V
Ring Centering Voltage	$V_{BH} = -75\text{V}$, $R_L = \infty$	-	-	± 3	V
	(Note 8)	-	-	-	V
AC TRANSMISSION PARAMETERS (Notes 5, 6)					
2-Wire Longitudinal Balance (Notes 11, 12)	Grade E	45	53	-	dB
	(Note 10)	-	-	-	dB
4-Wire Longitudinal Balance	Grade E	-	58	-	dB
	(Note 10)	-	-	-	dB
2-Wire to 4-Wire Level Linearity 4-Wire to 2-Wire Level Linearity Referenced to -10dBm	+3 to -40dBm, 1kHz	-	± 0.025	-	dB
	-40 to -50dBm, 1kHz	-	± 0.050	-	dB
	-50 to -55dBm, 1kHz	-	± 0.100	-	dB
DC PARAMETERS					
Loop Current Accuracy (Notes 5, 6)	$I_L = 25\text{mA}$	-	-	± 10	%
Open Circuit Voltage ((Tip - Ring), Note 6)	$V_{BL} = -16\text{V}$	-	7.5	-	V
	$V_{BL} = -24\text{V}$	14	15.5	17	V
	$V_{BH} = -60\text{V}$, BSEL = 1	43	50	-	V
Low Power Standby Open Circuit Voltage (Tip - Ring, Note 2)	$V_{BH} = -48\text{V}$	43	-	47	V
	$V_{BH} = -60\text{V}$, BSEL = 1	43	49	-	V
Absolute Open Circuit Voltage (Note 6)	V_{RG} in LPS and FA	-	-53	-56	V
	V_{TG} in RA	-	-	-	
	$V_{BH} = -60\text{V}$, BSEL = 1	-	-	-	
TEST ACCESS FUNCTIONS					
Switch On Voltage	(Note 13)	-	-	-	V
Loopback Max Battery	(Note 14)	-	-	52	V
SUPPLY CURRENTS (Supply currents not listed are considered negligible and do not contribute significantly to total power dissipation. All measurements made under open circuit load conditions.)					
Low Power Standby (Note 2)	I_{CC}	-	3.7	6.0	mA
	I_{BH} , $V_{BH} = -75\text{V}$	-	0.375	-	mA
Forward or Reverse (Note 5)	I_{CC}	2.0	4.0	6.0	mA
	I_{BL}	-	1.0	2.5	mA

HC55183, HC55184

Electrical Specifications Unless Otherwise Specified, $T_A = 0^\circ\text{C}$ to 70°C , $V_{BL} = -24\text{V}$, $V_{CC} = +5\text{V}$, $AGND = BGND = 0\text{V}$, loop current limit = 25mA. All AC Parameters are specified at 600Ω 2-wire terminating impedance over the frequency band of 300Hz to 3.4kHz. Protection resistors = 0Ω. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward (Note 2)	I_{CC}	2.0	5.5	8.0	mA
	I_{BL}	-	1.3	2.5	mA
	I_{BH} , $V_{BH} = -75\text{V}$	-	1.4	3.0	mA
Ringing (Note 2)	I_{CC}	-	8.5	-	mA
	I_{BL}	-	0.4	2.0	mA
	I_{BH} , $V_{BH} = -75\text{V}$	-	1.3	2.5	mA
Forward Loopback (Note 5)	(Note 14)	-	-	-	mA
		-	-	-	mA
Tip Open (Note 5)	(Note 15)	-	-	-	mA
		-	-	-	mA
Power Denial (Note 5)	I_{CC}	-	3.0	6.0	mA
	I_{BL}	-	0.2	0.5	mA
ON HOOK POWER DISSIPATION (Note 16)					
Forward or Reverse (Note 5, 6)	$V_{BL} = -24\text{V}$	-	44	60	mW
Low Power Standby (Note 2)	$V_{BH} = -75\text{V}$	-	46	70	mW
	(Note 8)	-	-	-	mW
Ringing (Note 2)	$V_{BH} = -75\text{V}$	-	170	275	mW
	(Note 8)	-	-	-	mW
OFF HOOK POWER DISSIPATION (Notes 5, 16)					
Forward or Reverse	$V_{BL} = -24\text{V}$	-	280	310	mW

NOTES:

7. Ringing Voltage is measured with $V_{RS} = 0.707 V_{RMS}$ for -85V devices and $V_{RS} = 0.619 V_{RMS}$ for -75V devices. All measurements are at $T = +25^\circ\text{C}$.
8. The HC55183 and HC55184 devices are specified with a single high battery voltage grade.
9. The device represents a low output impedance during ringing. Therefore the voltage across the ringing load is determined by the voltage divider formed by the protection resistance, loop resistance and ringing load impedance.
10. The HC55183 and HC55184 are specified with a single longitudinal balance grade.
11. Longitudinal Balance is tested per IEEE455-1985, with 368Ω per Tip and Ring Terminal.
12. These parameters are tested 100% at room temperature. These parameters are guaranteed not tested across temperature via statistical characterization.
13. The HC55183 and HC55184 do not support uncommitted switch operation.
14. The HC55183 and HC55184 do not support the Forward Loopback operating mode.
15. The HC55183 and HC55184 do not support the Tip Open operating mode.
16. The power dissipation numbers are actual device measurements and will be less than worst case calculations based on data sheet supply current limits.
17. Characterized with $2 \times 10\mu\text{s}$, and $10 \times 1000\mu\text{s}$ first level lightning surge waveforms (GR-1089-CORE).

Design Equations

Loop Supervision Thresholds

SWITCH HOOK DETECT

The switch hook detect threshold is set by a single external resistor, R_{SH} . Equation 1 is used to calculate the value of R_{SH} .

$$R_{SH} = 600/I_{SH} \quad (\text{EQ. 1})$$

The term I_{SH} is the desired DC loop current threshold. The loop current threshold programming range is from 5mA to 15mA.

GROUND KEY DETECT

The ground key detector senses a DC current imbalance between the Tip and Ring terminals when the ring terminal is connected to ground. The ground key detect threshold is not externally programmable and is internally fixed to 12mA regardless of the switch hook threshold.

RING TRIP DETECT

The ring trip detect threshold is set by a single external resistor, R_{RT} . I_{RT} should be set between the peak ringing current and the peak off hook current while still ringing.

$$R_{RT} = 1800/I_{RT} \quad (\text{EQ. 2})$$

The capacitor C_{RT} , in parallel with R_{RT} , will set the ring trip response time.

Loop Current Limit

The loop current limit of the device is programmed by the external resistor R_{IL} . The value of R_{IL} can be calculated using Equation 3.

$$R_{IL} = \frac{1760}{I_{LIM}} \quad (\text{EQ. 3})$$

The term I_{LIM} is the desired loop current limit. The loop current limit programming range is from 15mA to 45mA.

Impedance Matching

The impedance of the device is programmed with the external component R_S . R_S is the gain setting resistor for the feedback amplifier that provides impedance matching. If complex impedance matching is required, then a complex network can be substituted for R_S .

RESISTIVE IMPEDANCE SYNTHESIS

The source impedance of the device, Z_O , can be calculated in Equation 4.

$$R_S = 400(Z_O) \quad (\text{EQ. 4})$$

The required impedance is defined by the terminating impedance and protection resistors as shown in Equation 5.

$$Z_O = Z_L - 2R_P \quad (\text{EQ. 5})$$

4-WIRE TO 2-WIRE GAIN

The 4-wire to 2-wire gain is defined as the receive gain. It is a function of the terminating impedance, synthesized impedance and protection resistors. Equation 6 calculates the receive gain, G_{42} .

$$G_{42} = -2 \left(\frac{Z_L}{Z_O + 2R_P + Z_L} \right) \quad (\text{EQ. 6})$$

When the device source impedance and protection resistors equals the terminating impedance, the receive gain equals unity.

2-WIRE TO 4-WIRE GAIN

The 2-wire to 4-wire gain (G_{24}) is the gain from tip and ring to the VTX output. The transmit gain is calculated in Equation 7.

$$G_{24} = - \left(\frac{Z_O}{Z_O + 2R_P + Z_L} \right) \quad (\text{EQ. 7})$$

When the protection resistors are set to zero, the transmit gain is -6dB.

TRANSYBRID GAIN

The transhybrid gain is defined as the 4-wire to 4-wire gain (G_{44}).

$$G_{44} = - \left(\frac{Z_O}{Z_O + 2R_P + Z_L} \right) \quad (\text{EQ. 8})$$

When the protection resistors are set to zero, the transhybrid gain is -6dB.

COMPLEX IMPEDANCE SYNTHESIS

Substituting the impedance programming resistor, R_S , with a complex programming network provides complex impedance synthesis.

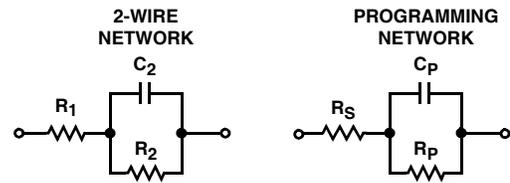


FIGURE 1. COMPLEX PROGRAMMING NETWORK

The reference designators in the programming network match the evaluation board. The component R_S has a different design equation than the R_S used for resistive impedance synthesis. The design equations for each component are provided in the following.

$$R_S = 400 \times (R_1 - 2(R_P)) \quad (\text{EQ. 9})$$

$$R_P = 400 \times R_2 \quad (\text{EQ. 10})$$

$$C_P = C_2/400 \quad (\text{EQ. 11})$$

Low Power Standby

Overview

The low power standby mode (LPS, 000) should be used during idle line conditions. The device is designed to operate from the high battery during this mode. Most of the internal circuitry is powered down, resulting in low power dissipation. If the 2-wire (tip/ring) DC voltage requirements are not critical during idle line conditions, the device may be operated from the low battery. Operation from the low battery will decrease the standby power dissipation.

TABLE 1. DEVICE INTERFACES DURING LPS

INTERFACE	ON	OFF	NOTES
Receive		x	AC transmission, impedance matching and ringing are disabled during this mode.
Ringing		x	
Transmit		x	
2-Wire	x		Amplifiers disabled.
Loop Detect	x		Switch hook or ground key.

2-Wire Interface

During LPS, the 2-wire interface is maintained with internal switches and voltage references. The Tip and Ring amplifiers are turned off to conserve power. The device will provide MTU compliance, loop current and loop supervision. Figure 2 represents the internal circuitry providing the 2-wire interface during low power standby.

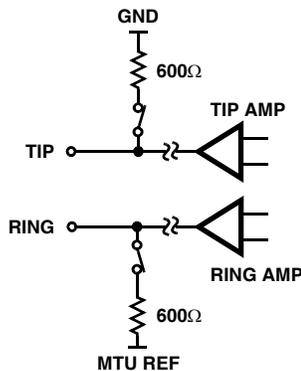


FIGURE 2. LPS 2-WIRE INTERFACE CIRCUIT DIAGRAM

MTU Compliance

Maintenance Termination Unit or MTU compliance places DC voltage requirements on the 2-wire terminals during idle line conditions. The minimum idle voltage is 42.75V. The high side of the MTU range is 56V. The voltage is expressed as the difference between Tip and Ring.

The Tip voltage is held near ground through a 600Ω resistor and switch. The Ring voltage is limited to a maximum of -49V (by MTU REF) when operating from either the high or low battery. A switch and 600Ω resistor connect the MTU reference to the Ring terminal. When the high battery

voltage exceeds the MTU reference of -49V (typically), the Ring terminal will be clamped by the internal reference. The same Ring relationships apply when operating from the low battery voltage. For high battery voltages (VBH) less than or equal to the internal MTU reference threshold:

$$V_{RING} = V_{BH} + 4 \quad (EQ. 12)$$

Loop Current

During LPS, the device will provide current to a load. The current path is through resistors and switches, and will be function of the off hook loop resistance (RLOOP). This includes the off hook phone resistance and copper loop resistance. The current available during LPS is determined by Equation 13.

$$I_{LOOP} = (-1 - (-49)) / (600 + 600 + R_{LOOP}) \quad (EQ. 13)$$

Internal current limiting of the standby switches will limit the maximum current to 20mA.

Another loop current related parameter is longitudinal current capability. The longitudinal current capability is reduced to 10mARMS per pin. The reduction in longitudinal current capability is a result of turning off the Tip and Ring amplifiers.

On Hook Power Dissipation

The on hook power dissipation of the device during LPS is determined by the operating voltages and quiescent currents and is calculated using Equation 14.

$$P_{LPS} = V_{BH} \times I_{BHQ} + V_{BL} \times I_{BLQ} + V_{CC} \times I_{CCQ} \quad (EQ. 14)$$

The quiescent current terms are specified in the electrical tables for each operating mode. Load power dissipation is not a factor since this is an on hook mode. Some applications may specify a standby current. The standby current may be a charging current required for modern telephone electronics.

Standby Current Power Dissipation

Any standby line current, ISLC, introduces an additional power dissipation term PSLC. Equation 15 illustrates the power contribution is zero when the standby line current is zero.

$$P_{SLC} = I_{SLC} \times (|V_{BH}| - 49 + 1 + I_{SLC} \times 1200) \quad (EQ. 15)$$

If the battery voltage is less than -49V (the MTU clamp is off), the standby line current power contribution reduces to Equation 16.

$$P_{SLC} = I_{SLC} \times (|V_{BH}| + 1 + I_{SLC} \times 1200) \quad (EQ. 16)$$

Most applications do not specify charging current requirements during standby. When specified, the typical charging current may be as high as 5mA.

Forward Active

Overview

The forward active mode (FA, 001) is the primary AC transmission mode of the device. On hook transmission, DC loop feed and voice transmission are supported during forward active. Loop supervision is provided by either the switch hook detector (E0 = 1) or the ground key detector (E0 = 0). The device may be operated from either high or low battery for on-hook transmission and low battery for loop feed.

On-Hook Transmission

The primary purpose of on hook transmission will be to support caller ID and other advanced signalling features. The transmission over load level while on hook is $3.5V_{PEAK}$.

When operating from the high battery, the DC voltages at Tip and Ring are MTU compliant. The typical Tip voltage is -4V and the Ring voltage is a function of the battery voltage for battery voltages less than -60V as shown in Equation 17.

$$V_{RING} = V_{BH} + 4 \quad (EQ. 17)$$

Loop supervision is provided by the switch hook detector at the \overline{DET} output. When \overline{DET} goes low, the low battery should be selected for DC loop feed and voice transmission.

Feed Architecture

The design implements a voltage feed current sense architecture. The device controls the voltage across Tip and Ring based on the sensing of load current. Resistors are placed in series with Tip and Ring outputs to provide the current sensing. The diagram below illustrates the concept.

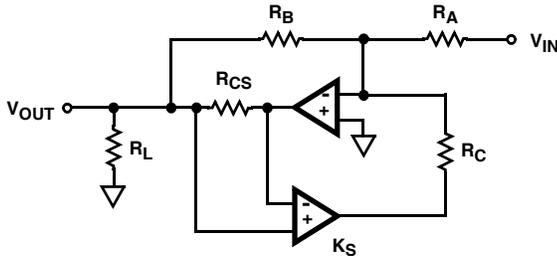


FIGURE 3. VOLTAGE FEED CURRENT SENSE DIAGRAM

By monitoring the current at the amplifier output, a negative feedback mechanism sets the output voltage for a defined load. The amplifier gains are set by resistor ratios (R_A , R_B , R_C) providing all the performance benefits of matched resistors. The internal sense resistor, R_{CS} , is much smaller than the gain resistors and is typically 20Ω for this device. The feedback mechanism, K_S , represents the amplifier configuration providing the negative feedback.

DC Loop Feed

The feedback mechanism for monitoring the DC portion of the loop current is the loop detector. A low pass filter is used in the feedback to block voice band signals from interfering with the loop current limit function. The pole of the low pass

filter is set by the external capacitor C_{DC} . The value of the external capacitor should be $4.7\mu F$.

Most applications will operate the device from low battery while off hook. The DC feed characteristic of the device will drive Tip and Ring towards half battery to regulate the DC loop current. For light loads, Tip will be near -4V and Ring will be near $V_{VBL} + 4V$. The following diagram shows the DC feed characteristic.

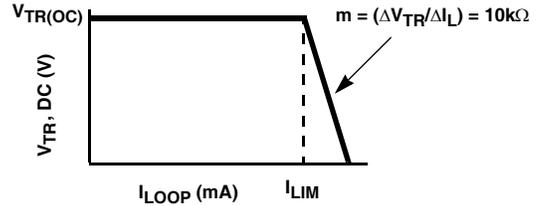


FIGURE 4. DC FEED CHARACTERISTIC

The point on the y-axis labeled $V_{TR(OC)}$ is the open circuit Tip to Ring voltage and is defined by the feed battery voltage.

$$V_{TR(OC)} = |V_{BL}| - 8 \quad (EQ. 18)$$

The curve of Figure 5 determines the actual loop current for a given set of loop conditions. The loop conditions are determined by the low battery voltage and the DC loop impedance. The DC loop impedance is the sum of the protection resistance, copper resistance (ohms/foot) and the telephone off hook DC resistance.

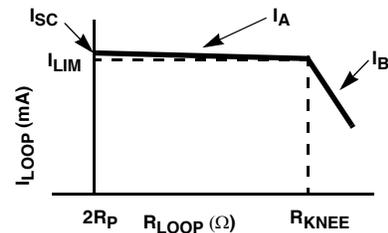


FIGURE 5. I_{LOOP} vs R_{LOOP} LOAD CHARACTERISTIC

The slope of the feed characteristic and the battery voltage define the maximum loop current on the shortest possible loop as the short circuit current I_{SC} .

$$I_{SC} = I_{LIM} + \frac{V_{TR(OC)} - 2R_P I_{LIM}}{10K} \quad (EQ. 19)$$

The term I_{LIM} is the programmed current limit, $1760/R_{IL}$. The line segment I_A represents the constant current region of the loop current limit function.

$$I_A = I_{LIM} + \frac{V_{TR(OC)} - R_{LOOP} I_{LIM}}{10K} \quad (EQ. 20)$$

The maximum loop impedance for a programmed loop current is defined as R_{KNEE} .

$$R_{KNEE} = \frac{V_{TR(OC)}}{I_{LIM}} \quad (EQ. 21)$$

When R_{KNEE} is exceeded, the device will transition from constant current feed to constant voltage, resistive feed. The line segment I_B represents the resistive feed portion of the load characteristic.

$$I_B = \frac{V_{TR(OC)}}{R_{LOOP}} \quad (EQ. 22)$$

Voice Transmission

The feedback mechanism for monitoring the AC portion of the loop current consists of two amplifiers, the sense amplifier (SA) and the transmit amplifier (TA). The AC feedback signal is used for impedance synthesis. A detailed model of the AC feed back loop is provided in the following.

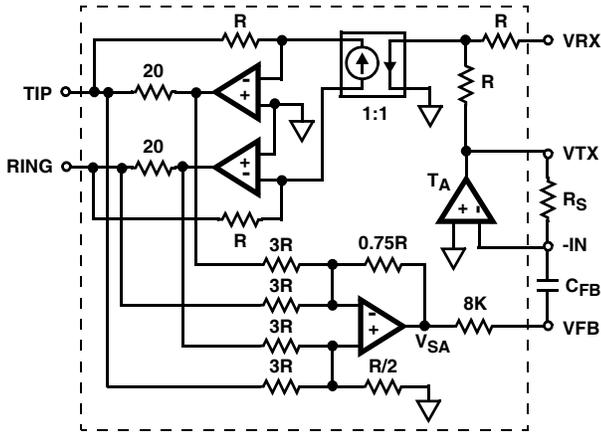


FIGURE 6. AC SIGNAL TRANSMISSION MODEL

The gain of the transmit amplifier, set by R_S , determines the programmed impedance of the device. The capacitor C_{FB} blocks the DC component of the loop current. The ground symbols in the model represent AC grounds, not actual DC potentials.

The sense amp output voltage, V_{SA} , as a function of Tip and Ring voltage and load is calculated using Equation 23.

$$V_{SA} = -(V_T - V_R) \frac{10}{Z_L} \quad (EQ. 23)$$

The transmit amplifier provides the programmable gain required for impedance synthesis. In addition, the output of this amplifier interfaces to the CODEC transmit input. The output voltage is calculated using Equation 24.

$$V_{VTX} = -V_{SA} \left(\frac{R_S}{8K} \right) \quad (EQ. 24)$$

Once the impedance matching components have been selected using the design equations, the above equations provide additional insight as to the expected AC node voltages for a specific Tip and Ring load.

Transhybrid Balance

The final step in completing the impedance synthesis design is calculating the necessary gains for transhybrid balance.

The AC feed back loop produces an echo at the V_{TX} output of the signal injected at V_{RX} . The echo must be cancelled to maintain voice quality. Most applications will use a summing amplifier in the CODEC front end as shown below to cancel the echo signal.

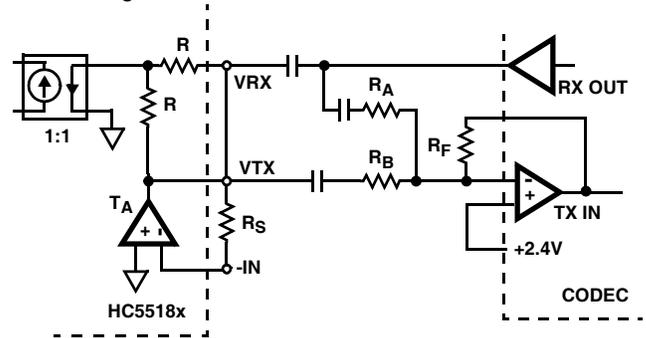


FIGURE 7. TRANSHYBRID BALANCE INTERFACE

The resistor ratio, R_F/R_B , provides the final adjustment for the transmit gain, G_{TX} . The transmit gain is calculated using Equation 25.

$$G_{TX} = -G_{24} \left(\frac{R_F}{R_B} \right) \quad (EQ. 25)$$

Most applications set $R_F = R_B$, hence the device 2-wire to 4-wire equals the transmit gain. Typically R_B is greater than 20kΩ to prevent loading of the device transmit output.

The resistor ratio, R_F/R_A , is determined by the transhybrid gain of the device, G_{44} . R_F is previously defined by the transmit gain requirement and R_A is calculated using Equation 26.

$$R_A = \frac{R_B}{G_{44}} \quad (EQ. 26)$$

Power Dissipation

The power dissipated by the device during on hook transmission is strictly a function of the quiescent currents for each supply voltage during Forward Active operation.

$$P_{FAQ} = V_{BH} \times I_{BHQ} + V_{BL} \times I_{BLQ} + V_{CC} \times I_{CCQ} \quad (EQ. 27)$$

Off hook power dissipation is increased above the quiescent power dissipation by the DC load. If the loop length is less than or equal to R_{KNEE} , the device is providing constant current, I_A , and the power dissipation is calculated using Equation 28.

$$P_{FA(IA)} = P_{FA(Q)} + (V_{BL} \times I_A) - (R_{LOOP} \times I_A^2) \quad (EQ. 28)$$

If the loop length is greater than R_{KNEE} , the device is operating in the constant voltage, resistive feed region. The power dissipated in this region is calculated using Equation 29.

$$P_{FA(IB)} = P_{FA(Q)} + (V_{BL} \times I_B) - (R_{LOOP} \times I_B^2) \quad (EQ. 29)$$

Since the current relationships are different for constant current versus constant voltage, the region of device operation is critical to valid power dissipation calculations.

Reverse Active

Overview

The reverse active mode (RA, 011) provides the same functionality as the forward active mode. On hook transmission, DC loop feed and voice transmission are supported. Loop supervision is provided by either the switch hook detector (E0 = 1) or the ground key detector (E0 = 0). The device may be operated from either high or low battery.

During reverse active the Tip and Ring DC voltage characteristics exchange roles. That is, Ring is typically 4V below ground and Tip is typically 4V more positive than battery. Otherwise, all feed and voice transmission characteristics are identical to forward active.

Silent Polarity Reversal

Changing from forward active to reverse active or vice versa is referred to as polarity reversal. Many applications require slew rate control of the polarity reversal event. Requirements range from minimizing cross talk to protocol signalling.

The device uses an external low voltage capacitor, C_{POL}, to set the reversal time. Once programmed, the reversal time will remain nearly constant over various load conditions. In addition, the reversal timing capacitor is isolated from the AC loop, therefore loop stability is not impacted.

The internal circuitry used to set the polarity reversal time is shown in the following.

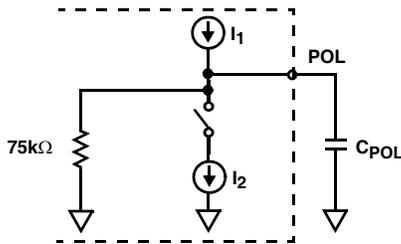


FIGURE 8. REVERSAL TIMING CONTROL

During forward active, the current from source I1 charges the external timing capacitor C_{POL} and the switch is open. The internal resistor provides a clamping function for voltages on the POL node. During reverse active, the switch closes and I2 (roughly twice I1) pulls current from I1 and the timing capacitor. The current at the POL node provides the drive to a differential pair which controls the reversal time of the Tip and Ring DC voltages.

$$C_{POL} = \frac{\Delta time}{75000} \tag{EQ. 30}$$

Where Δtime is the required reversal time. Polarized capacitors may be used for C_{POL}. The low voltage at the POL pin and minimal voltage excursion ±0.75V, are well suited to polarized capacitors.

Power Dissipation

The power dissipation equations for forward active operation also apply to the reverse active mode.

Ringing

Overview

The ringing mode (RNG, 100) provides linear amplification to support a variety of ringing waveforms. A programmable ring trip function provides loop supervision and auto disconnect upon ring trip. The device is designed to operate from the high battery during this mode.

Architecture

The device provides linear amplification to the signal applied to the ringing input, V_{RS}. The differential ringing gain of the device is 80V/V. The circuit model for the ringing path is shown in the following figure.

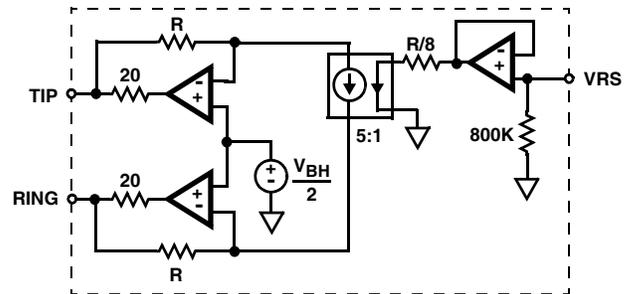


FIGURE 9. LINEAR RINGING MODEL

The voltage gain from the VRS input to the Tip output is 40V/V. The resistor ratio provides a gain of 8 and the current mirror provides a gain of 5. The voltage gain from the VRS input to the Ring output is -40V/V. The equations for the Tip and Ring outputs during ringing are provided below.

$$V_T = \frac{V_{BH}}{2} + (40 \times VRS) \tag{EQ. 31}$$

$$V_R = \frac{V_{BH}}{2} - (40 \times VRS) \tag{EQ. 32}$$

When the input signal at VRS is zero, the Tip and Ring amplifier outputs are centered at half battery. The device provides auto centering for easy implementation of sinusoidal ringing waveforms. Both AC and DC control of the Tip and Ring outputs is available during ringing. This feature allows for DC offsets as part of the ringing waveform.

Ringing Input

The ringing input, V_{RS}, is a high impedance input. The high impedance allows the use of low value capacitors for AC coupling the ring signal. The V_{RS} input is enabled only during the ringing mode, therefore a free running oscillator may be connected to VRS at all times.

When operating from a battery of -75V, each amplifier, Tip and Ring, will swing a maximum of 70V_{p-p}. Hence, the maximum signal swing at VRS to achieve full scale ringing is

approximately 2.4V_{P-P}. The low signal levels are compatible with the output voltage range of the CODEC. The digital nature of the CODEC ideally suits it for the function of programmable ringing generator. See Applications.

Logic Control

Ringing patterns consist of silent intervals. The ringing to silent pattern is called the ringing cadence. During the silent portion of ringing, the device can be programmed to any other operating mode. The most likely candidates are low power standby or forward active. Depending on system requirements, the low or high battery may be selected.

Loop supervision is provided with the ring trip detector. The ring trip detector senses the change in loop current when the phone is taken off hook. The loop detector full wave rectifies the ringing current, which is then filtered with external components R_{RT} and C_{RT}. The resistor R_{RT} sets the trip threshold and the capacitor C_{RT} sets the trip response time. Most applications will require a trip response time less than 150ms.

Three very distinct actions occur when the devices detects a ring trip. First, the \overline{DET} output is latched low. The latching mechanism eliminates the need for software filtering of the detector output. The latch is cleared when the operating mode is changed externally. Second, the VRS input is disabled, removing the ring signal from the line. Third, the device is internally forced to the forward active mode.

Power Dissipation

The power dissipation during ringing is dictated by the load driving requirements and the ringing waveform. The key to valid power calculations is the correct definition of average and RMS currents. The average current defines the high battery supply current. The RMS current defines the load current.

The cadence provides a time averaging reduction in the peak power. The total power dissipation consists of ringing power, P_r, and the silent interval power, P_s.

$$P_{RNG} = P_r \times \frac{t_r}{t_r + t_s} + P_s \times \frac{t_s}{t_r + t_s} \quad (EQ. 33)$$

The terms t_r and t_s represent the cadence. The ringing interval is t_r and the silent interval is t_s. The typical cadence ratio t_r:t_s is 1:2.

The quiescent power of the device in the ringing mode is defined in Equation 34.

$$P_{r(Q)} = V_{BH} \times I_{BHQ} + V_{BL} \times I_{BLQ} + V_{CC} \times I_{CCQ} \quad (EQ. 34)$$

The total power during the ringing interval is the sum of the quiescent power and loading power:

$$P_r = P_{r(Q)} + V_{BH} \times I_{AVG} - \frac{V_{RMS}^2}{Z_{REN} + R_{LOOP}} \quad (EQ. 35)$$

For sinusoidal waveforms, the average current, I_{AVG}, is defined in Equation 36.

$$I_{AVG} = \left(\frac{2}{\pi}\right) \frac{V_{RMS} \times \sqrt{2}}{Z_{REN} + R_{LOOP}} \quad (EQ. 36)$$

The silent interval power dissipation will be determined by the quiescent power of the selected operating mode.

Forward Loop Back

Overview

The forward loop back mode (FLB, 101) provides test capability for the device. An internal signal path is enabled allowing for both DC and AC verification. The internal 600Ω terminating resistor has a tolerance of ±20%. The device is intended to operate from only the low battery during this mode.

Architecture

When the forward loop back mode is initiated internal switches connect a 600Ω load across the outputs of the Tip and Ring amplifiers.

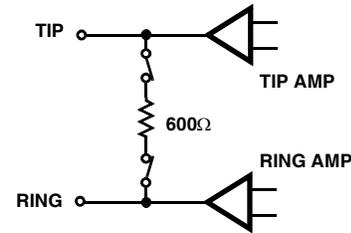


FIGURE 10. FORWARD LOOP BACK INTERNAL TERMINATION

DC Verification

When the internal signal path is provided, DC current will flow from Tip to Ring. The DC current will force \overline{DET} low, indicating the presence of loop current. In addition, the \overline{ALM} output will also go low. This does not indicate a thermal alarm condition. Rather, proper logic operation is verified in the event of a thermal shutdown. In addition to verifying device functionality, toggling the logic outputs verifies the interface to the system controller.

AC Verification

The entire AC loop of the device is active during the forward loop back mode. Therefore a 4-wire to 4-wire level test capability is provided. Depending on the transhybrid balance implementation, test coverage is provided by a one or two step process.

System architectures which cannot disable the transhybrid function would require a two step process. The first step would be to send a test tone to the device while on hook and not in forward loop back mode. The return signal would be the test level times the gain R_F/R_A of the transhybrid amplifier. Since the device would not be terminated, cancellation would not occur. The second step would be to program the device to FLB and resend the test tone. The

return signal would be much lower in amplitude than the first step, indicating the device was active and the internal termination attenuated the return signal.

System architectures which disable the transhybrid function would achieve test coverage with a signal step. Once the transhybrid function is disabled, program the device for FLB and send the test tone. The return signal level is determined by the 4-wire to 4-wire gain of the device.

Tip Open

Overview

The tip open mode (110) is intended for compatibility for PBX type interfaces. Used during idle line conditions, the device does not provide transmission. Loop supervision is provided by either the switch hook detector ($E0 = 1$) or the ground key detector ($E0 = 0$). The ground key detector will be used in most applications. The device may be operated from either high or low battery.

Functionality

During tip open operation, the Tip amplifier is disabled and the Ring amplifier is enabled. The minimum Tip impedance is $30k\Omega$. The only active path through the device will be the Ring amplifier.

In keeping with the MTU characteristics of the device, Ring will not exceed $-56.5V$ when operating from the high battery. Though MTU does not apply to tip open, safety requirements are satisfied.

On Hook Power Dissipation

The on hook power dissipation of the device during tip open is determined by the operating voltages and quiescent currents and is calculated using Equation 37.

$$P_{TO} = V_{BH} \times I_{BHQ} + V_{BL} \times I_{BLQ} + V_{CC} \times I_{CCQ} \quad (\text{EQ. 37})$$

The quiescent current terms are specified in the electrical tables for each operating mode. Load power dissipation is not a factor since this is an on hook mode.

Power Denial

Overview

The power denial mode (111) will shutdown the entire device except for the logic interface. Loop supervision is not provided. This mode may be used as a sleep mode or to shut down in the presence of a persistent thermal alarm. Switching between high and low battery will have no effect during power denial.

Functionality

During power denial, both the Tip and Ring amplifiers are disabled, representing high impedances. The voltages at both outputs are near ground.

Thermal Shutdown

In the event the safe die temperature is exceeded, the \overline{ALM} output will go low and \overline{DET} will go high and the part will automatically shut down. When the device cools, \overline{ALM} will go high and \overline{DET} will reflect the loop status. If the thermal fault persists, \overline{ALM} will go low again and the part will shut down. Programming power denial will permanently shutdown the device and stop the self cooling cycling.

Battery Switching

Overview

The integrated battery switch selects between the high battery and low battery. The battery switch is controlled with the logic input BSEL. When BSEL is a logic high, the high battery is selected and when a logic low, the low battery is selected. All operating modes of the device will operate from high or low battery except forward loop back.

Functionality

The logic control is independent of the operating mode decode. Independent logic control provides the most flexibility and will support all application configurations.

When changing device operating states, battery switching should occur simultaneously with or prior to changing the operating mode. In most cases, this will minimize overall power dissipation and prevent glitches on the DET output.

The only external component required to support the battery switch is a diode in series with the V_{BH} supply lead. In the event that high battery is removed, the diode allows the device to transition to low battery operation.

Low Battery Operation

All off hook operating conditions should use the low battery. The prime benefit will be reduced power dissipation. The typical low battery for the device is $-24V$. However this may be increased to support longer loop lengths or high loop current requirements. Standby conditions may also operate from the low battery if MTU compliance is not required, further reducing standby power dissipation.

High Battery Operation

Other than ringing, the high battery should be used for standby conditions which must provide MTU compliance. During standby operation the power consumption is typically less than $50mW$ with $-75V$ battery. If ringing requirements do not require full $75V$ operation, then a lower battery will result in lower standby power.

High Voltage Decoupling

The $75V$ rating of the device will require a capacitor of higher voltage rating for decoupling. Suggested decoupling values for all device pins are $0.1\mu F$. Standard surface mount ceramic capacitors are rated at $100V$. For applications driven at low cost and small size, the decoupling scheme shown below could be implemented.

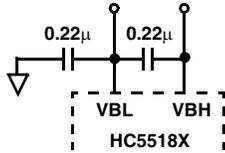


FIGURE 11. ALTERNATE DECOUPLING SCHEME

As with all decoupling schemes, the capacitors should be as close to the device pins as physically possible.

Uncommitted Switch

Overview

The uncommitted switch is a three terminal device designed for flexibility. The independent logic control input, SWC, allows switch operation regardless of device operating mode. The switch is activated by a logic low. The positive and negative terminals of the device are labeled SW+ and SW- respectively.

Relay Driver

The uncommitted switch may be used as a relay driver by connecting SW+ to the relay coil and SW- to ground. The switch is designed to have a maximum on voltage of 0.6V with a load current of 45mA.

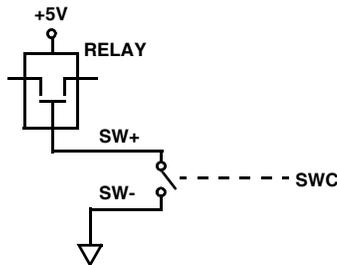


FIGURE 12. EXTERNAL RELAY SWITCHING

Since the device provides the ringing waveform, the relay functions which may be supported include subscriber disconnect, test access or line interface bypass. An external snubber diode is not required when using the uncommitted switch as a relay driver.

Test Load

The switch may be used to connect test loads across Tip and Ring. The test loads can provide external test termination for the device. Proper connection of the uncommitted switch to Tip and Ring is shown in the following.

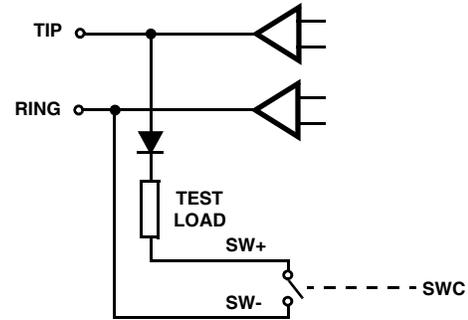


FIGURE 13. TEST LOAD SWITCHING

The diode in series with the test load blocks current from flowing through the uncommitted switch when the polarity of the Tip and Ring terminals are reversed. In addition to the reverse active state, the polarity of Tip and Ring are reversed for half of the ringing cycle. With independent logic control and the blocking diode, the uncommitted switch may be continuously connected to the Tip and Ring terminals.

Basic Application Circuits

TABLE 2. BASIC APPLICATION CIRCUIT COMPONENT LIST

COMPONENT	VALUE	TOLERANCE	RATING
U1 - Ringing SLIC	HC5518x	N/A	N/A
R _{RT}	20kΩ	1%	0.1W
R _{SH}	49.9kΩ	1%	0.1W
R _{IL}	71.5kΩ	1%	0.1W
R _S	210kΩ	1%	0.1W
C _{RX} , C _{RS} , C _{TX} , C _{RT} , C _{POL} , C _{FB}	0.47μF	20%	10V
C _{DC}	4.7μF	20%	10V
C _{PS1}	0.1μF	20%	>100V
C _{PS2} , C _{PS3}	0.1μF	20%	100V
D ₁	1N400X type with breakdown > 100V.		
R _{P1} , R _{P2}	Protection resistor values are application dependent and will be determined by protection requirements. Standard applications will use ≥ 35Ω per side.		

Design Parameters: Ring Trip Threshold = 90mA_{PEAK}, Switch Hook Threshold = 12mA, Loop Current Limit = 24.6mA, Synthesize Device Impedance = 210kΩ/400 = 525Ω, with 39Ω protection resistors, impedance across Tip and Ring terminals = 603Ω. Where applicable, these component values apply to the Basic Application Circuits for the HC55183 and HC55184. Pins not shown in the Basic Application Circuit are no connect (NC) pins.

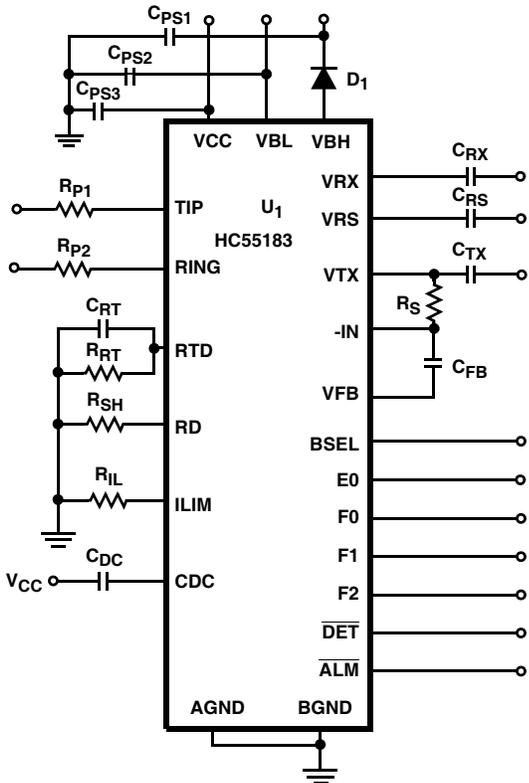


FIGURE 14. HC55183 BASIC APPLICATION CIRCUIT

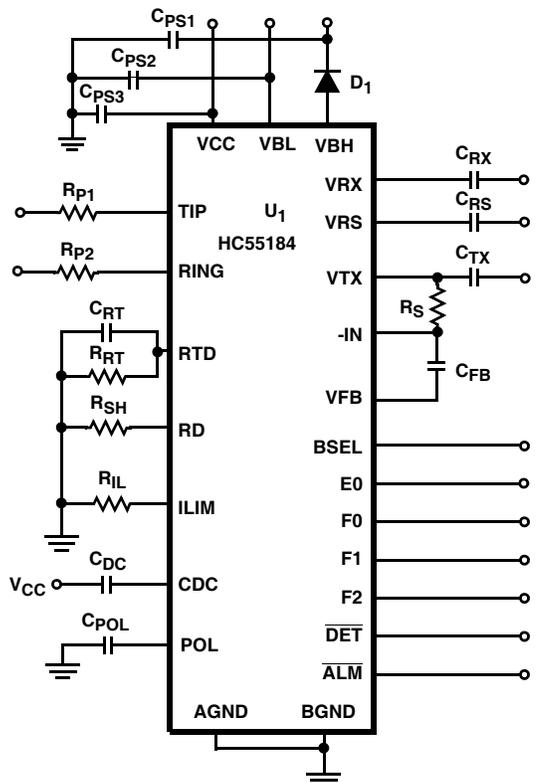


FIGURE 15. HC55184 BASIC APPLICATION CIRCUIT

Additional Application Diagrams

Reducing Overhead Voltages

The transmission overhead voltage of the device is internally set to 4V per side. The overhead voltage may be reduced by injecting a negative DC voltage on the receive input using a voltage divider (Figure 16). Accordingly, the 2-wire port overload level will decrease the same amount as the injected offset.

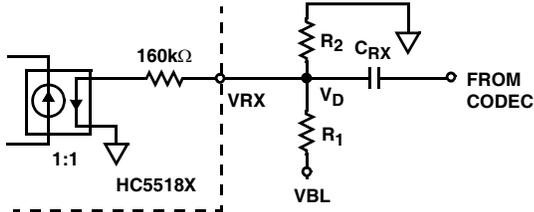


FIGURE 16. EXTERNAL OVERHEAD CONTROL

The divider shunt resistance is the parallel combination of the internal 160kΩ resistor and the external R₂. The sum of R₁ and R₂ should be greater than 500kΩ to minimize the additional power dissipation of the divider. The DC gain relationship from the divider voltage, V_D, to the Tip and Ring outputs is shown below.

$$V_{T-R} = |V_{BL}| - 8 - (2 \times V_D) \tag{EQ. 38}$$

With a low battery voltage -24V and a divider voltage of -0.5V, the Tip to Ring voltage is 17V. As a result, the overhead voltage is reduced from 8V to 7V and the overload level will decrease from 3.5V_{PEAK} to 3.0V_{PEAK}.

CODEC Ringing Generation

Maximum ringing amplitudes of the device are achieved with signal levels approximately 2.4V_{p-p}. Therefore the low pass receive output of the CODEC may serve as the low level ring generator. The ringing input impedance of 480kΩ minimum should not interfere with CODEC drive capability. A single external capacitor is required to AC couple the ringing signal from the CODEC. The circuit diagram for CODEC ringing is shown below.

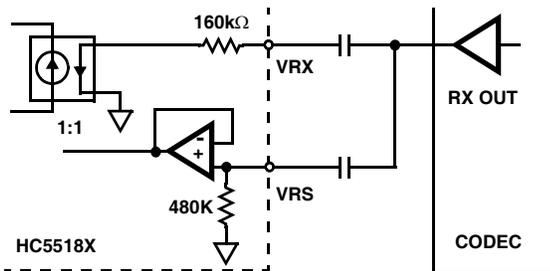


FIGURE 17. CODEC RINGING INTERFACE

Implementing Teletax Signalling

A resistor, R_T, is required at the -IN input of the device for injecting the teletax signal (Figure 17). For most

applications the synthesized device impedance (i.e., 600Ω) will not match the 200Ω teletax impedance. The gain set by R_T cancels the impedance matching feedback with respect to the teletax injection point. Therefore the device appears as a low impedance source for teletax. The resistor R_T is calculated using the following equation.

$$R_T = \frac{200}{200 + 2 \times R_P + (R_S/400)} \times R_S \tag{EQ. 39}$$

The signal level across a 200Ω load will be twice the injected teletax signal level. As the teletax level at VTX will equal the injection level, set R_C = R_B for cancellation. The value of R_B is based on the voice band transhybrid balance requirements. The connection of the teletax source to the transhybrid amplifier should be AC coupled to allow proper biasing of the transhybrid amplifier input

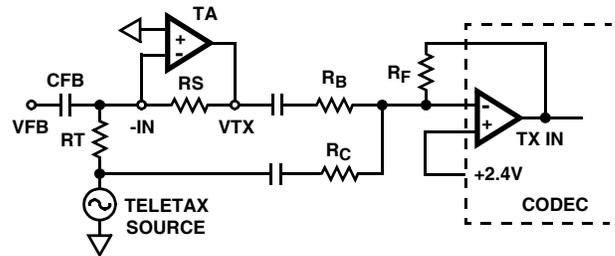


FIGURE 18. TELETAX SIGNALLING

Ringing With DC Offsets

The balanced ringing waveform consists of zero DC offset between the Tip and Ring terminals. However, the linear amplifier architecture provides control of the DC offset during ringing. The DC gain is the same as the AC gain, 40V/V per amplifier. Positive DC offsets applied directly to the ringing input will shift both Tip and Ring away from half battery towards ground and battery respectively. A voltage divider on the ringing input may be used to generate the offset (Figure 19). The reference voltage, V_{REF}, can be either the CODEC 2.4V reference voltage or the 5V supply.

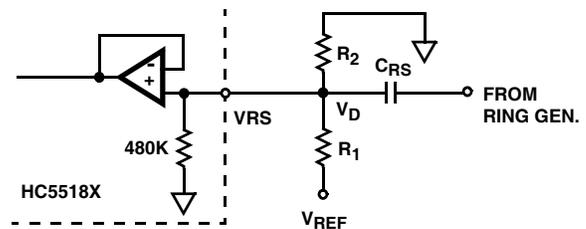


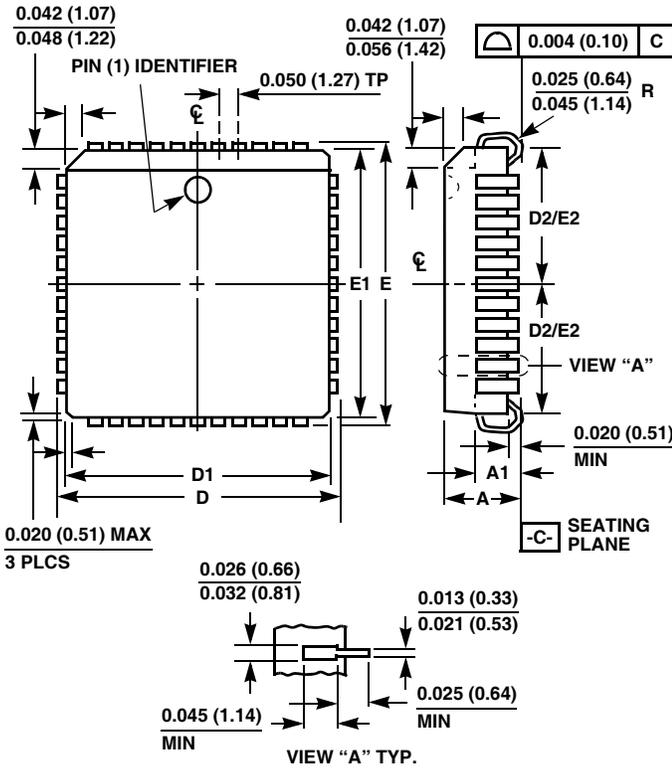
FIGURE 19. EXTERNAL OVERHEAD CONTROL

An offset during ringing of 30V, would require a DC shift of 15V at Tip and 15V at Ring. The DC offset would be created by a +0.375V (V_D) at the VRS input. The divider resistors should be selected to minimize the value of the AC coupling capacitor C_{RS} and the loading of the ring generator and voltage reference. The ringing input impedance should also be accounted for in divider resistor calculations.

Pin Descriptions

PLCC	SYMBOL	DESCRIPTION
1	TIP	TIP power amplifier output.
2	BGND	Battery Ground - To be connected to zero potential. All loop current and longitudinal current flow from this ground. Internally separate from AGND but it is recommended that it is connected to the same potential as AGND.
3	VBL	Low battery supply connection.
4	VBH	High battery supply connection for the most negative battery.
5, 6, 7, 16	NC	No connect
8	F2	Mode control input - MSB. F2-F0 for the TTL compatible parallel control interface for controlling the various modes of operation of the device.
9	F1	Mode control input.
10	F0	Mode control input.
11	E0	Detector Output Selection Input. This TTL input controls the multiplexing of the SHD (E0 = 1) and GKD (E0 = 0) comparator outputs to the \overline{DET} output based upon the state at the F2-F0 pins (see the Device Operating Modes table shown on page 2).
12	\overline{DET}	Detector Output - This TTL output provides on-hook/off-hook status of the loop based upon the selected operating mode. The detected output will either be switch hook, ground key or ring trip (see the Device Operating Modes table shown on page 2).
13	\overline{ALM}	Thermal Shutdown Alarm. This pin signals the internal die temperature has exceeded safe operating temperature (approximately 175°C) and the device has been powered down automatically.
14	AGND	Analog ground reference. This pin should be externally connected to BGND.
15	BSEL	Selects between high and low battery, with a logic "1" selecting the high battery and logic "0" the low battery. This pin is a no connect (NC) on the HC55180.
17	POL	External capacitor on this pin sets the polarity reversal time. This pin is a no connect on the HC55183.
18	VRS	Ringing Signal Input - Analog input for driving 2-wire interface while in Ring Mode.
19	VRX	Analog Receive Voltage - 4-wire analog audio input voltage. AC couples to CODEC.
20	VTX	Transmit output voltage - Output of impedance matching amplifier, AC couples to CODEC.
21	VFB	Feedback voltage for impedance matching. This voltage is scaled to accomplish impedance matching.
22	-IN	Impedance matching amplifier summing node.
23	VCC	Positive voltage power supply, usually +5V.
24	CDC	DC Biasing Filter Capacitor - Connects between this pin and VCC.
25	RTD	Ring trip filter network.
26	ILIM	Loop Current Limit programming resistor.
27	RD	Switch hook detection threshold programming resistor.
28	RING	RING power amplifier output.

Plastic Leaded Chip Carrier Packages (PLCC)



N28.45 (JEDEC MS-018AB ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D1	0.450	0.456	11.43	11.58	3
D2	0.191	0.219	4.86	5.56	4, 5
E	0.485	0.495	12.32	12.57	-
E1	0.450	0.456	11.43	11.58	3
E2	0.191	0.219	4.86	5.56	4, 5
N	28		28		6

Rev. 2 11/97

NOTES:

- Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
- Dimensions and tolerancing per ANSI Y14.5M-1982.
- Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
- To be measured at seating plane -C- contact point.
- Centerline to be determined where center leads exit plastic body.
- "N" is the number of terminal positions.

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