CMS45P03H8-HF

Description

The CMS45P03H8-HF is the highest performance trench P-ch MOSFET with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

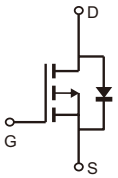
The CMS45P03H8-HF meet the RoHS and Green Product requirement,100% EAS guaranteed with full function reliability approved.

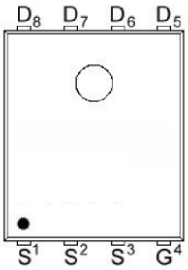
Features

- •Advanced DMOS trench technology
- •Improve dv/dt capability
- •Green device available
- •Fast switching
- •100% EAS guaranteed

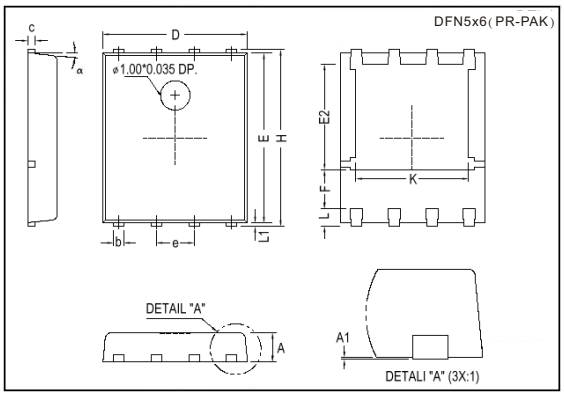
Circuit diagram

- G : Gate
- S : Source
- D : Drain





Package Dimensions



REF.	Millimeter			REF.	Millimeter		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	0.85	1.00	1.15	E	5.70	-	5.90
A1	0.00	-	0.10	e	-	1.27	-
b	0.30	-	0.51	H	5.90	-	6.20
c	0.20	-	0.30	L	-	0.60	-
D	4.80	-	5.00	L1	0.06	-	0.20
F	1.10REF.			α	0°	-	12°
E2	3.50REF.			K	3.70	3.90	4.10

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current[1]	I_D @T_C=25℃	-45	A
	I_D @T_C=100℃	-30	A
Pulsed Drain Current[1,2]	I_{DM}	-150	A
Continuous Drain Current[1]	I_D @T_A=25℃	-9.6	A
	I_D @T_A=70℃	-7.7	A
Total Power Dissipation[4]	P_D @T_C=25℃	45	W
	P_D @T_A=25℃	2	W
Single Pulse Avalanche Energy, L=0.1mH[3]	E_{AS}	88	mJ
Single Pulse Avalanche Current, L=0.1mH[3]	I_{AS}	-42	A
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 ~ +150	℃

Thermal Data

Parameter	Symbol	Conditions	Max. Value	Unit
Thermal Resistance Junction-ambient[1]	$R_{\theta JA}$	Steady State	62.5	℃/W
Thermal Resistance Junction-case[1]	$R_{\theta JC}$	Steady State	2.8	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	-30	-	-	V	V_{GS}=0 , I_D=250uA
Gate Threshold Voltage	$V_{GS(th)}$	-1.0	-	-2.5	V	V_{DS}=V_{GS} , I_D=250uA
Forward Transconductance	gfs	-	30	-	S	V_{DS}=-5V , I_D=-30A
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}=±20V
Drain-Source Leakage Current(T_J=25℃)	I_{DSS}	-	-	-1	uA	V_{DS}=-30V , V_{GS}=0
Drain-Source Leakage Current(T_J=55℃)		-	-	-5		V_{DS}=-24V , V_{GS}=0
Static Drain-Source On-Resistance[2]	$R_{DS(ON)}$	-	-	15	mΩ	V_{GS}=-10V , I_D=30A
		-	-	25		V_{GS}=-4.5V , I_D=15A
Total Gate Charge[2]	Q_g	-	22	-	nC	I_D=-15A
Gate-Source Charge	Q_{gs}	-	8.7	-		V_{DS}=-15V
Gate-Drain (“Miller”) Change	Q_{gd}	-	7.2	-		V_{GS}=-4.5V
Turn-on Delay Time[2]	$T_{d(on)}$	-	8	-	ns	V_{DD}=-15V
Rise Time	T_r	-	73.7	-		I_D=-15A
Turn-off Delay Time	$T_{d(off)}$	-	61.8	-		V_{GS}=-10V
Fall Time	T_f	-	24.4	-		R_G=3.3Ω
Input Capacitance	C_{iss}	-	2215	-	pF	V_{GS}=0V
Output Capacitance	C_{oss}	-	310	-		V_{DS}=-15V
Reverse Transfer Capacitance	C_{rss}	-	237	-		f=1.0MHz
Gate Resistance	R_g	-	9	-	Ω	f=1.0MHz

Guaranteed Avalanche Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Single Pulse Avalanche Energy[5]	EAS	22	-	-	mJ	V_{DD}=-25V, L=0.1mH, I_{AS}=-21A

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward on Voltage[2]	V_{SD}	-	-	-1.2	V	I_S=-30A , V_{GS}=0V , T_J=25℃
Continuous Source Current[1,6]	I_S	-	-	-45	A	V_G=V_D=0V , Force Current
Pulsed Source Current[2,6]	I_{SM}	-	-	-150	A	
Reverse Recovery Time	trr	-	19	-	ns	I_F=-15A,dI/dt=100A/μs
Reverse Recovery Charge	Qrr	-	9	-	nC	T_J=25℃

Notes: 1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2.The data tested by pulsed,pulse width ≤ 300us,duty cycle ≤ 2%.

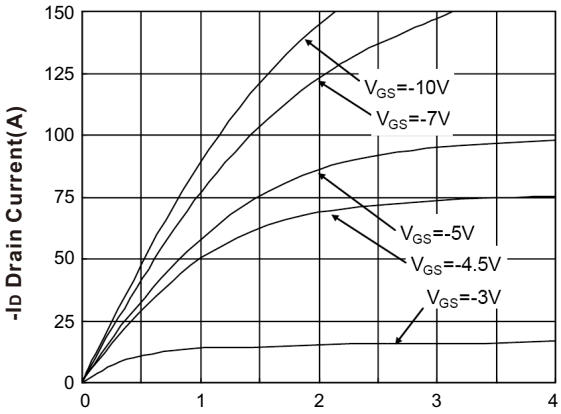
3.The EAS data shows Max. rating. The test condition is V_{DD}=-25V,V_{GS}=-10V,L=0.1mH,I_{AS}=-42A.

4.The power dissipation is limited by 150℃ junction temperature.

5.The Min. Value is 100% EAS tested guarantee.

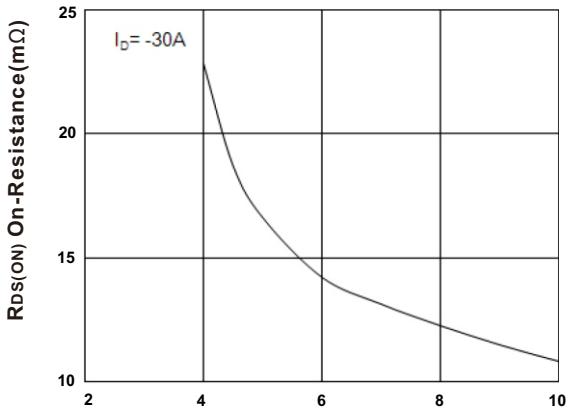
6.The data is theoretically the same as ID and IDM,in real applications,should be limited by total power dissipation.

Typical Characteristics



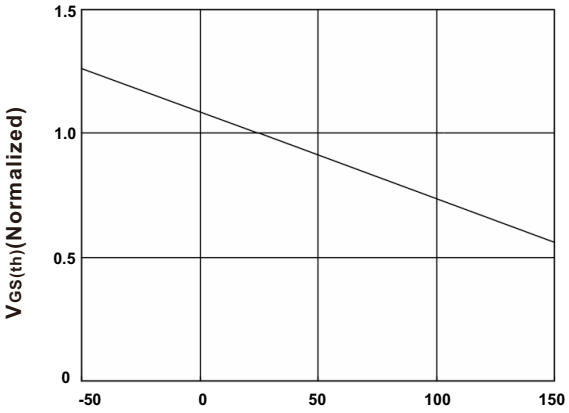
-VDS Drain-to-Source Voltage (V)

Fig.1 Typical Output Characteristics



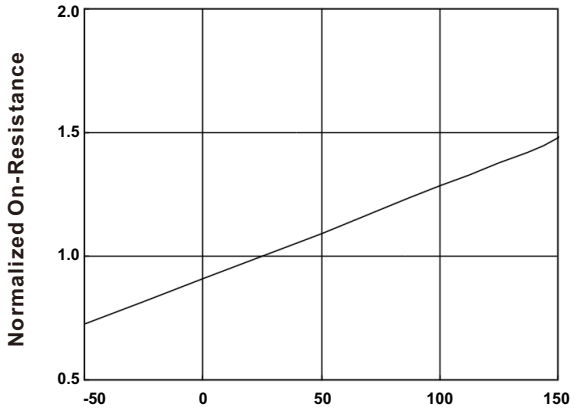
-VGS Gate-to-source Voltage (V)

Fig.2 On-Resistance vs. G-S Voltage



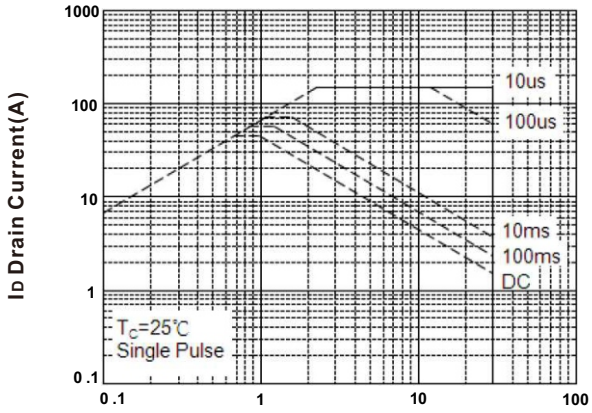
TJ Junction Temperature (℃)

Fig. 3 Normalized VGS(th) VS. TJ



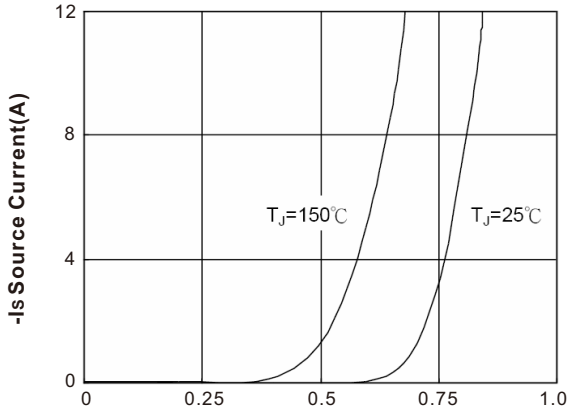
TJ Junction Temperature (℃)

Fig. 4 Normalized RDSON vs. TJ



-VDS Drain-to-source Voltage (V)

Fig. 5 Safe Operating Area



-VSD Source-to-Drain Voltage (V)

Fig. 6 Forward Characteristics of Reverse

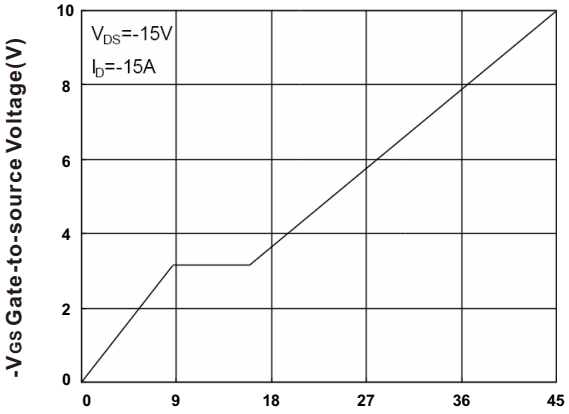


Fig.7 Gate Charge Characteristics

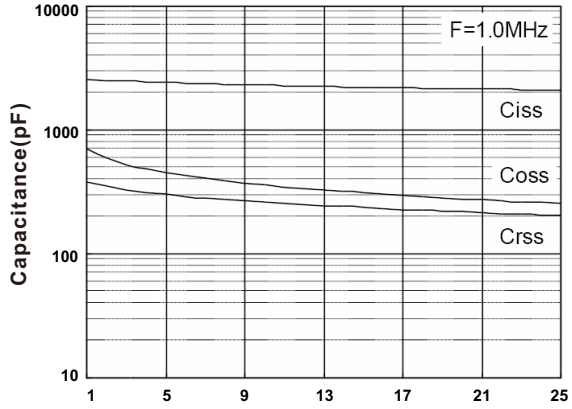


Fig.8 Capacitance Characteristics

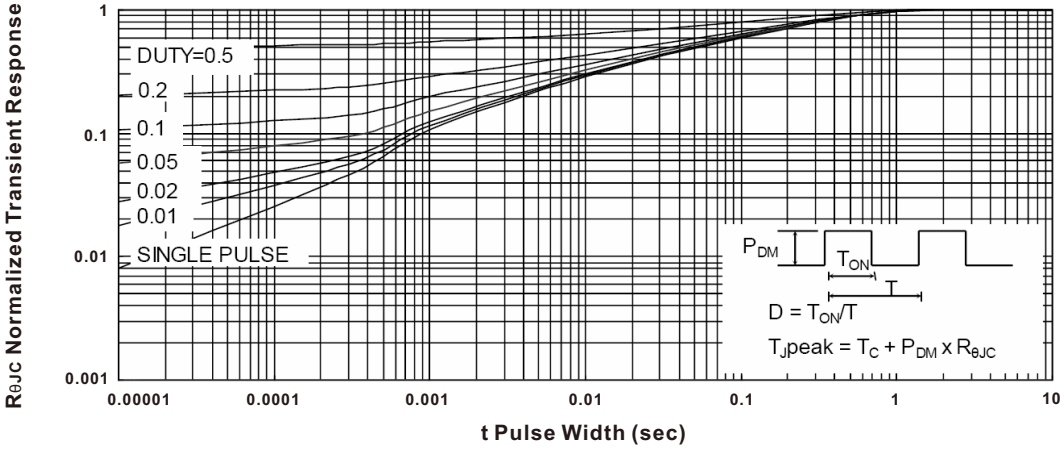


Fig.9 Normalized Maximum Transient Thermal Impedance

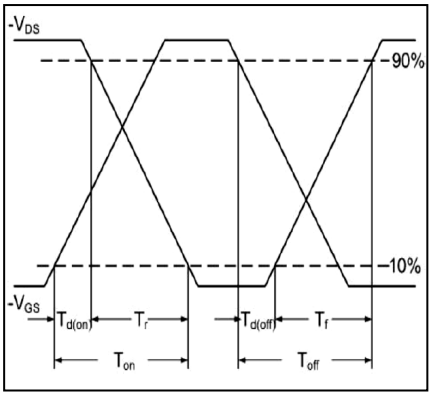


Fig. 10 Switching Time Waveform

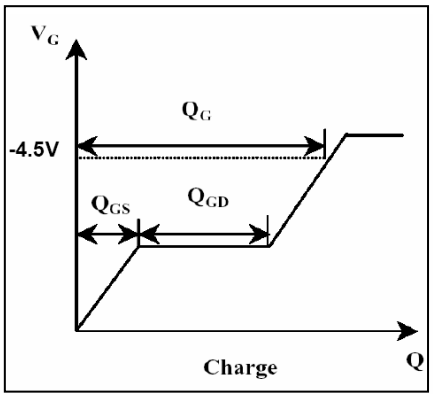
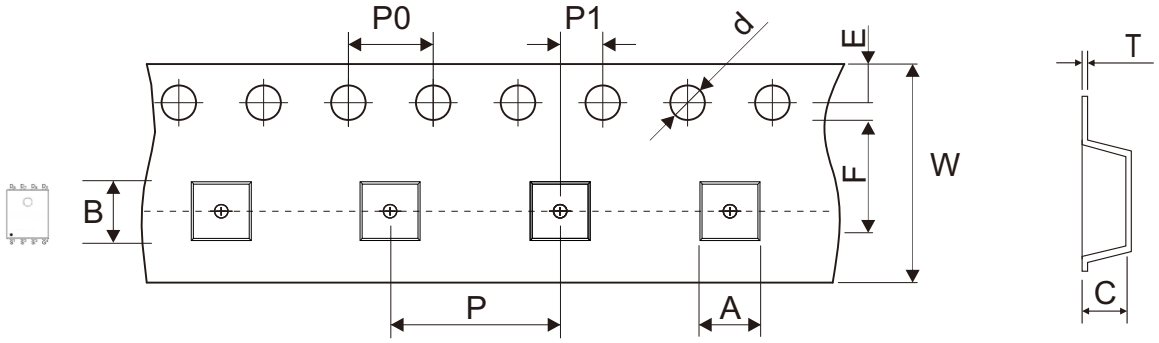
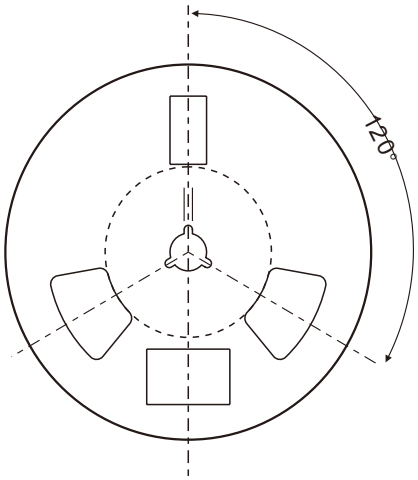
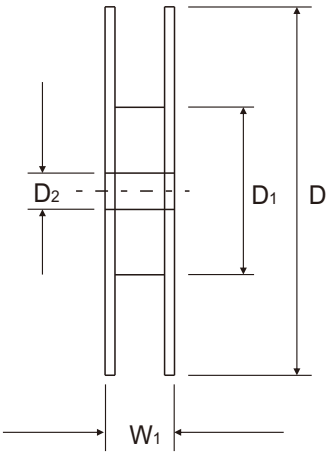


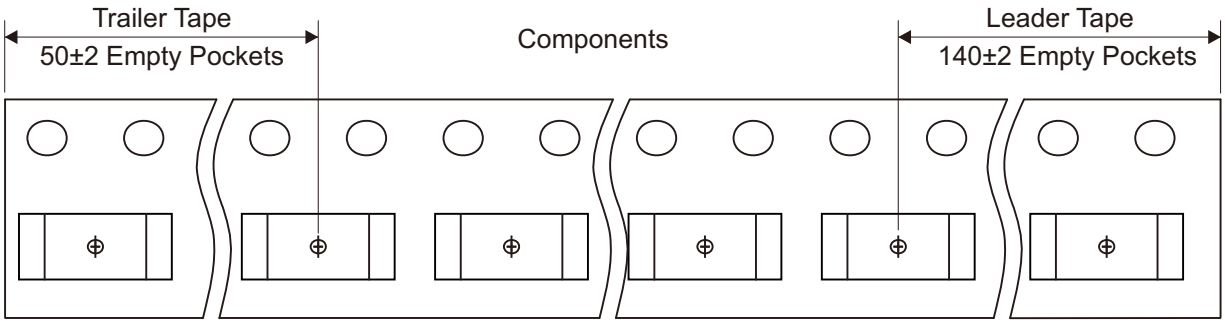
Fig. 11 Gate Charge Waveform

Reel Taping Specification







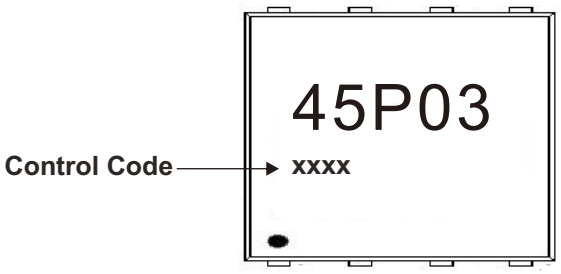


	Symbol	A	B	C	d	D	D_1	D_2
DFN5x6 (PR-PAK)	(mm)	6.50 ± 0.10	5.30 ± 0.10	1.40 ± 0.10	1.50 ± 0.05	330.00 ± 2.00	178.00 ± 2.00	13.00 ± 1.00
	(inch)	0.256 ± 0.004	0.209 ± 0.004	0.055 ± 0.004	0.059 ± 0.002	12.992 ± 0.079	7.008 ± 0.079	0.512 ± 0.039

	Symbol	E	F	P	P0	P1	T	W	W1
DFN5x6 (PR-PAK)	(mm)	1.75 ± 0.10	5.50 ± 0.05	8.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.05	0.30 ± 0.05	12.00 ± 0.30	18.40 ± 1.00
	(inch)	0.069 ± 0.004	0.217 ± 0.002	0.315 ± 0.004	0.157 ± 0.004	0.079 ± 0.002	0.012 ± 0.002	0.472 ± 0.012	0.724 ± 0.039

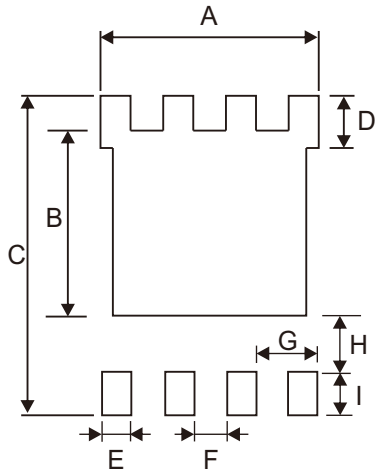
Marking Code

Part Number	Marking Code
CMS45P03H8	45P03



Suggested PAD Layout

Dimensions	Value (in mm)
A	4.420
B	3.810
C	6.610
D	1.020
E	0.610
F	0.660
G	1.270
H	0.820
I	1.270



Note:

1.The pad layout is for reference purposes only.

Standard Packaging

Case Type	REEL PACK	
	REEL (pcs)	Reel Size (inch)
DFN5x6 (PR-PAK)	3,000	13