# Integrated Power Solution with Quad Low Noise Buck Regulators

Data Sheet

# ADP5014

## FEATURES

- Input voltage range: 2.75 V to 6.0 V
- Programmable output voltage range: 0.5 V to 0.9 × PVINx
- Low output noise: ~25 µV rms when $V_{OUT} \leq V_{REF}$
- ±1.0% output accuracy over full temperature range
- 500 kHz to 2.5 MHz adjustable switching frequency
- Power regulation
  - Channel 1 and Channel 2: programmable 2 A/4 A sync buck regulators, or single 8 A output in parallel
  - Channel 3 and Channel 4: programmable 1 A/2 A sync buck regulators, or single 4 A output in parallel
- Flexible parallel operation
- Precision enable with 0.6 V threshold
- Manual or sequence mode for power-up and power-down sequence
- Selective FPWM or PSM operation mode
- Precision undervoltage comparator
- Frequency synchronization input or output
- Active output discharge switch
- Power-good flag on selective channels via factory fuse
- UVLO, OVP, OCP, and TSD protection
- 40-lead, 6 mm × 6 mm LFCSP package
- –40°C to +125°C junction temperature

## APPLICATIONS

- RF transceiver, high speed analog-to-digital converter (ADC)/digital-to-analog converter (DAC), mixed signal ASIC
- FPGA and processor applications
- Security and surveillance
- Medical applications

## TYPICAL APPLICATION CIRCUIT

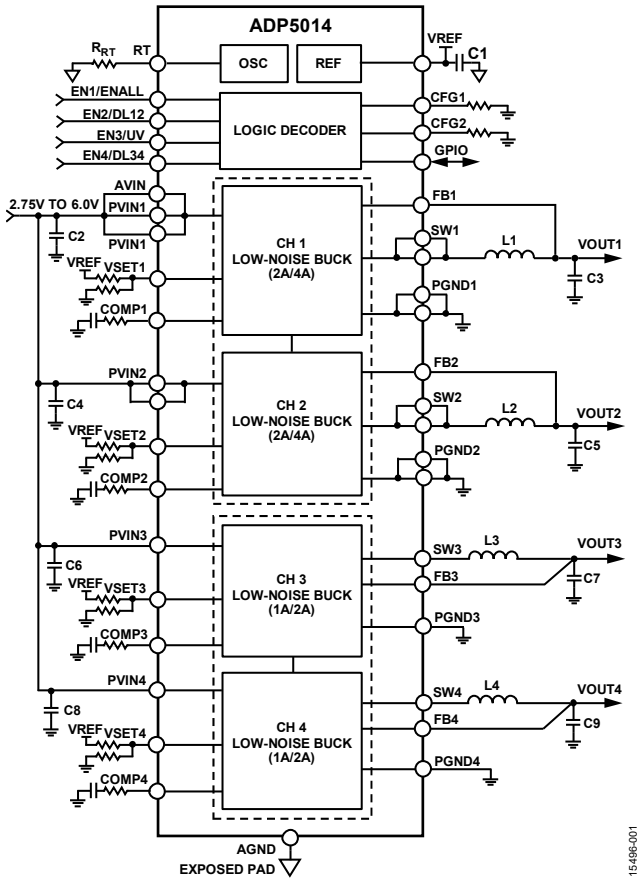


*Figure 1.*

## GENERAL DESCRIPTION

The ADP5014 combines four high performance, low noise buck regulators in a 40-lead LFCSP package. Relying on its low output noise (~25 µV rms when $V_{OUT} \leq V_{REF}$), the low noise buck regulator enables the powering up of the noise sensitive signal chain products.

All channels in the ADP5014 integrate high-side and low-side power metal-oxide semiconductor field effect transistors (MOSFET). Channel 1 and Channel 2 deliver a programmable output current of 2 A or 4 A. Combining Channel 1 and Channel 2 in a parallel configuration provides a single output with up to 8 A of current.

Channel 3 and Channel 4 deliver a programmable output current of 1 A or 2 A. Combining Channel 3 and Channel 4 in a parallel configuration can provide a single output with up to 4 A of current.

The ADP5014 features two enable modes. The manual mode has four individual precision enable pins to enable each regulator manually. Alternatively, the sequence mode has one grouped precision enable signal with programmable power-up and power-down delay timers on each rail for specific rail sequence requirements.

The switching frequency of the ADP5014 can be programmed or synchronized to an external clock from 500 kHz to 2.5 MHz.

The ADP5014 offers other key features like selective forced pulse width modulation (FPWM)/power saving mode (PSM), an undervoltage output (UVO), active output discharge, and a power-good flag. Other safety features include input undervoltage lockout (UVLO), overvoltage protection (OVP), overcurrent protection (OCP) and thermal shutdown (TSD).


**Rev. A** Document Feedback




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# DETAILED FUNCTIONAL BLOCK DIAGRAM

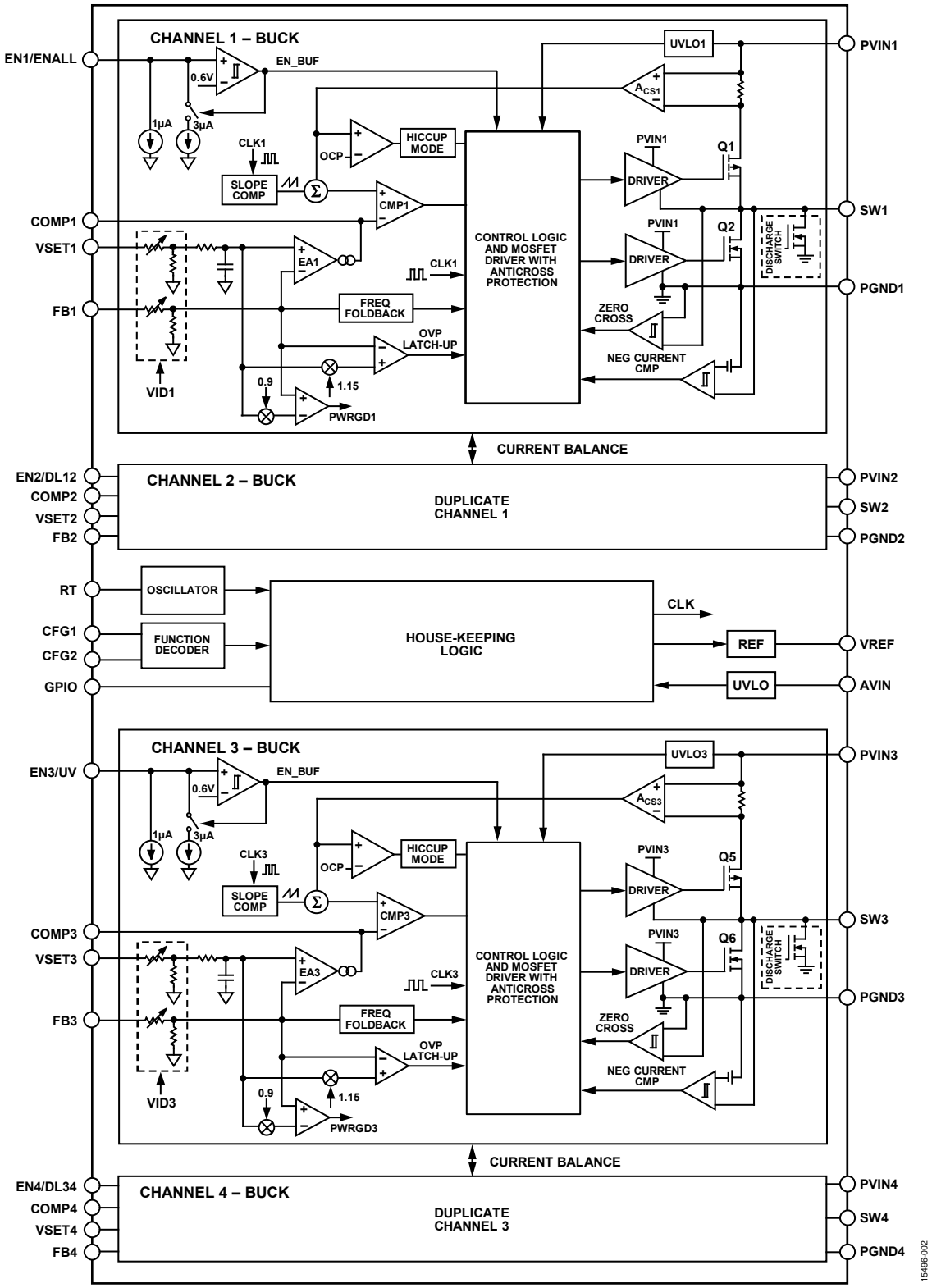



*Figure 2.*

# SPECIFICATIONS

$V_{IN}$ = 5 V, $T_J$ = −40°C to +125°C for minimum and maximum specifications, and $T_A$ = 25°C for typical specifications, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| INPUT SUPPLY VOLTAGE RANGE | $V_{IN}$ | 2.75 | | 6.0 | V | AVIN, PVIN1, PVIN2, PVIN3, PVIN4 pins |
| QUIESCENT CURRENT | | | | | | AVIN, PVIN1, PVIN2, PVIN3, PVIN4 pins |
| Operating Quiescent Current | $I_Q$ | | 5.4 | 7.0 | mA | No switching, all ENx pins high |
| Shutdown Current | $I_{SHDN}$ | | 47 | 85 | µA | All ENx pins low |
| UNDERVOLTAGE LOCKOUT | UVLO | | | | | AVIN, PVIN1, PVIN2, PVIN3, PVIN4 pins |
| Threshold, Rising | $V_{UVLO-RISING}$ | | 2.65 | 2.75 | V | |
| Threshold, Falling | $V_{UVLO-FALLING}$ | 2.30 | 2.40 | | V | |
| Hysteresis | $V_{HYS}$ | | 0.25 | | V | |
| REFERENCE | | | | | | |
| Output Voltage | $V_{REF}$ | | 2.0 | | V | |
| Accuracy | | −1.0 | | +1.0 | % | |
| Maximum Load | | 1 | | | mA | |
| OSCILLATOR CIRCUIT | | | | | | |
| Switching Frequency Range | | 500 | | 2500 | kHz | |
| Switching Frequency | $f_{SW}$ | 1000 | 1200 | 1400 | kHz | $R_{RT}$ = 82.5 kΩ |
| Sync Input | | | | | | |
| Input Clock Range | $f_{SYNC}$ | 500 | | 2500 | kHz | |
| Input Clock Pulse Width | | | | | | |
| Minimum On Time | $t_{SYNC\_MIN\_ON}$ | 100 | | | ns | |
| Minimum Off Time | $t_{SYNC\_MIN\_OFF}$ | 100 | | | ns | |
| Input Clock High Voltage | $V_{H(SYNC)}$ | 1.3 | | | V | |
| Input Clock Low Voltage | $V_{L(SYNC)}$ | | | 0.4 | V | |
| Sync Output | | | | | | |
| Clock Frequency | $f_{CLK}$ | | $f_{SW}$ | | kHz | |
| Positive Pulse Duty Cycle | $t_{CLK\_PULSE\_DUTY}$ | | 50 | | % | |
| Rise or Fall Time | $t_{CLK\_RISE\_FALL}$ | | 10 | | ns | |
| High Level Voltage | $V_{H(SYNC\_OUT)}$ | | $V_{AVIN}$ | | V | |
| PRECISION ENABLING | | | | | | EN1, EN2, EN3, EN4 pins |
| High Level Threshold | $V_{TH\_H(EN)}$ | | 0.6 | 0.65 | V | |
| Low Level Threshold | $V_{TH\_L(EN)}$ | 0.52 | 0.57 | | V | |
| Source Current | $I_{TH\_L(EN)}$ | | 4 | | µA | Below the falling threshold |
| DELAY TIMER | | | | | | |
| Programmable Delay Timer Range | $t_{DELAY}$ | 6 | | 48 | ms | |
| Delay Timer | $t_{DELAY}$ | | 6 | | ms | Timer ×1 option |
| | | | 48 | | ms | Timer ×8 option |
| POWER GOOD | | | | | | |
| Internal Power-Good Rising Threshold | $V_{PWRGD(RISE)}$ | 87 | 90 | 93 | % | |
| Internal Power-Good Hysteresis | $V_{PWRGD(HYS)}$ | | 3 | | % | |
| Internal Power-Good Falling Delay | $t_{PWRGD\_FALL}$ | | 50 | | µs | |
| Rising Delay for PWRGD Pin | $t_{PWRGD\_PIN\_RISE}$ | | 2 | | ms | Timer ×1 option |
| | | | 16 | | ms | Timer ×8 option |
| Leakage Current for PWRGD Pin | $I_{PWRGD\_LEAKAGE}$ | | 0.1 | 1 | µA | |
| Output Low Voltage for PWRGD Pin | $V_{PWRGD\_LOW}$ | | 70 | 150 | mV | $I_{PWRGD}$ = 1 mA |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| THERMAL SHUTDOWN | | | | | | |
| Thermal Shutdown Threshold | $T_{SHDN}$ | | 150 | | °C | |
| Thermal Shutdown Hysteresis | $T_{HYS}$ | | 15 | | °C | |

## BUCK REGULATOR SPECIFICATIONS

$V_{IN}$ = 5 V, $f_{SW}$ = 1.2 MHz for all channels, $T_J$ = −40°C to +125°C for minimum and maximum specifications, and $T_A$ = 25°C for typical specifications, unless otherwise noted.

**Table 2.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| CHANNEL 1 SYNC BUCK REGULATOR | | | | | | |
| Load Current | $I_{LOAD1}$ | | | 4 | A | |
| Output Characteristics | | | | | | |
| $V_{FB1}$ Voltage Accuracy | | | | | | −40°C ≤ $T_J$ ≤ +125°C |
| | $V_{FB1}$ | −0.6 | | +0.6 | % | $V_{SET1} = V_{REF}$ |
| | | −1.0 | | +1.0 | % | $V_{SET1} = ½ \times V_{REF}$ |
| Feedback Bias Current | $I_{FB1}$ | | | 0.1 | µA | |
| VSET1 Bias Current | $I_{VSET1}$ | | | 0.1 | µA | |
| SW1 Pin | | | | | | |
| High-Side Power Field Effect Transistor (FET) On Resistance | $R_{DS(ON)1H}$ | | 49 | 80 | mΩ | Pin to pin measurement |
| Low-Side Power FET On Resistance | $R_{DS(ON)1L}$ | | 37 | 60 | mΩ | Pin to pin measurement |
| Current-Limit Threshold | $I_{TH(ILIM1)}$ | 5.2 | 6.9 | 8.6 | A | $R_{CFG1}$ = 0 kΩ |
| | | 2.5 | 3.5 | 4.5 | A | $R_{CFG1}$ = 17.8 kΩ |
| Minimum On Time | $t_{MIN\_ON1}$ | | 60 | 90 | ns | $f_{SW}$ = 500 kHz to 2.5 MHz |
| Minimum Off Time | $t_{MIN\_OFF1}$ | | 50 | 80 | ns | $f_{SW}$ = 500 kHz to 2.5 MHz |
| Error Amplifier, COMP1 Pin | | | | | | |
| EA Transconductance | $g_{m1}$ | 700 | 800 | 900 | µS | |
| Soft Start Time | $t_{SS1}$ | | 2 | | ms | Timer ×1 option |
| | | | 16 | | ms | Timer ×8 option |
| Programmable Soft Start Range | | 2 | | 16 | ms | |
| Hiccup Time | $t_{HICCUP1}$ | | 7 × $t_{SS1}$ | | ms | |
| $C_{OUT}$ Discharge Switch On Resistance | $R_{DIS1}$ | | 85 | | Ω | |
| CHANNEL 2 SYNC BUCK REGULATOR | | | | | | |
| Load Current | $I_{LOAD2}$ | | | 4 | A | |
| Output Characteristics | | | | | | |
| $V_{FB2}$ Voltage Accuracy | | | | | | −40°C ≤ $T_J$ ≤ +125°C |
| | $V_{FB2}$ | −0.6 | | +0.6 | % | $V_{SET2} = V_{REF}$ |
| | | −1.0 | | +1.0 | % | $V_{SET2} = ½ \times V_{REF}$ |
| Feedback Bias Current | $I_{FB2}$ | | | 0.1 | µA | |
| VSET2 Bias Current | $I_{VSET2}$ | | | 0.1 | µA | |
| SW2 Pin | | | | | | |
| High-Side Power FET On Resistance | $R_{DS(ON)2H}$ | | 49 | 80 | mΩ | Pin to pin measurement |
| Low-Side Power FET On Resistance | $R_{DS(ON)2L}$ | | 37 | 60 | mΩ | Pin to pin measurement |
| Current-Limit Threshold | $I_{TH(ILIM2)}$ | 5.2 | 6.9 | 8.6 | A | $R_{CFG1}$ = 0 kΩ |
| | | 2.5 | 3.5 | 4.5 | A | $R_{CFG1}$ = 17.8 kΩ |
| Minimum On Time | $t_{MIN\_ON2}$ | | 60 | 90 | ns | $f_{SW}$ = 500 kHz to 2.5 MHz |
| Minimum Off Time | $t_{MIN\_OFF2}$ | | 50 | 80 | ns | $f_{SW}$ = 500 kHz to 2.5 MHz |
| Error Amplifier, COMP2 Pin | | | | | | |
| Transconductance | $g_{m2}$ | 700 | 800 | 900 | µS | |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| Soft Start Time | $t_{SS2}$ | | 2 | | ms | Timer ×1 option |
| | | | 16 | | ms | Timer ×8 option |
| Programmable Soft Start Range | | 2 | | 16 | ms | |
| Hiccup Time | $t_{HICCUP2}$ | | 7 × $t_{SS2}$ | | ms | |
| $C_{OUT}$ Discharge Switch On Resistance | $R_{DIS2}$ | | 85 | | Ω | |
| CHANNEL 3 SYNC BUCK REGULATOR | | | | | | |
| Load Current | $I_{LOAD3}$ | | | 2 | A | |
| Output Characteristics | | | | | | |
| $V_{FB3}$ Voltage Accuracy | | | | | | −40°C ≤ $T_J$ ≤ +125°C |
| | $V_{FB3}$ | −0.6 | | +0.6 | % | $V_{SET3} = V_{REF}$ |
| | | −1.0 | | +1.0 | % | $V_{SET3} = ½ \times V_{REF}$ |
| Feedback Bias Current | $I_{FB3}$ | | | 0.1 | µA | |
| VSET3 Bias Current | $I_{VSET3}$ | | | 0.1 | µA | |
| SW3 Pin | | | | | | |
| High-Side Power FET On Resistance | $R_{DS(ON)3H}$ | | 95 | 135 | mΩ | Pin to pin measurement |
| Low-Side Power FET On Resistance | $R_{DS(ON)3L}$ | | 73 | 110 | mΩ | Pin to pin measurement |
| Current-Limit Threshold | $I_{TH(ILIM3)}$ | 2.5 | 3.5 | 4.5 | A | $R_{CFG1}$ = 0 kΩ |
| | | 1.2 | 1.8 | 2.4 | A | $R_{CFG1}$ = 17.8 kΩ |
| Minimum On Time | $t_{MIN\_ON3}$ | | 60 | 90 | ns | $f_{SW}$ = 500 kHz to 2.5 MHz |
| Minimum Off Time | $t_{MIN\_OFF3}$ | | 50 | 80 | ns | $f_{SW}$ = 500 kHz to 2.5 MHz |
| Error Amplifier, COMP3 Pin | | | | | | |
| EA Transconductance | $g_{m3}$ | 700 | 800 | 900 | µS | |
| Soft Start Time | $t_{SS3}$ | | 2 | | ms | Timer ×1 option |
| | | | 16 | | ms | Timer ×8 option |
| Programmable Soft Start Range | | 2 | | 16 | ms | |
| Hiccup Time | $t_{HICCUP3}$ | | 7 × $t_{SS3}$ | | ms | |
| $C_{OUT}$ Discharge Switch On Resistance | $R_{DIS3}$ | | 85 | | Ω | |
| CHANNEL 4 SYNC BUCK REGULATOR | | | | | | |
| Load Current | $I_{LOAD4}$ | | | 2 | A | |
| Output Characteristics | | | | | | |
| $V_{FB4}$ Voltage Accuracy | | | | | | −40°C ≤ $T_J$ ≤ +125°C |
| | $V_{FB4}$ | −0.6 | | +0.6 | % | $V_{SET4} = V_{REF}$ |
| | | −1.0 | | +1.0 | % | $V_{SET4} = ½ \times V_{REF}$ |
| Feedback Bias Current | $I_{FB4}$ | | | 0.1 | µA | |
| VSET4 Bias Current | $I_{VSET4}$ | | | 0.1 | µA | |
| SW4 Pin | | | | | | |
| High-Side Power FET On Resistance | $R_{DS(ON)4H}$ | | 95 | 135 | mΩ | Pin to pin measurement |
| Low-Side Power FET On Resistance | $R_{DS(ON)4L}$ | | 73 | 110 | mΩ | Pin to pin measurement |
| Current-Limit Threshold | $I_{TH(ILIM4)}$ | 2.5 | 3.5 | 4.5 | A | $R_{CFG1}$ = 0 kΩ |
| | | 1.2 | 1.8 | 2.4 | A | $R_{CFG1}$ = 17.8 kΩ |
| Minimum On Time | $t_{MIN\_ON4}$ | | 60 | 90 | ns | $f_{SW}$ = 500 kHz to 2.5 MHz |
| Minimum Off Time | $t_{MIN\_OFF4}$ | | 50 | 80 | ns | $f_{SW}$ = 500 kHz to 2.5 MHz |
| Error Amplifier, COMP4 Pin | | | | | | |
| EA Transconductance | $g_{m4}$ | 700 | 800 | 900 | µS | |
| Soft Start Time | $t_{SS4}$ | | 2 | | ms | Timer ×1 option |
| | | | 16 | | ms | Timer ×8 option |
| Programmable Soft Start Range | | 2 | | 16 | ms | |
| Hiccup Time | $t_{HICCUP4}$ | | 7 × $t_{SS4}$ | | ms | |
| $C_{OUT}$ Discharge Switch On Resistance | $R_{DIS4}$ | | 85 | | Ω | |

# ABSOLUTE MAXIMUM RATINGS

**Table 3.**

| Parameter | Rating |
|---|---|
| AVIN to Ground | −0.3 V to +6.5 V |
| PVIN1 to PGND1 | −0.3 V to +6.5 V |
| PVIN2 to PGND2 | −0.3 V to +6.5 V |
| PVIN3 to PGND3 | −0.3 V to +6.5 V |
| PVIN4 to PGND4 | −0.3 V to +6.5 V |
| SW1 to PGND1 | −0.3 V to +6.5 V |
| SW2 to PGND2 | −0.3 V to +6.5 V |
| SW3 to PGND3 | −0.3 V to +6.5 V |
| SW4 to PGND4 | −0.3 V to +6.5 V |
| PGND to Ground | −0.3 V to + 0.3 V |
| CFG1, CFG2 to Ground | −0.3 V to +6.5 V |
| EN1/ENALL, EN2/DL12, EN3/UV, EN4/DL34 to Ground | −0.3 V to +6.5 V |
| GPIO to Ground | −0.3 V to +6.5 V |
| RT to Ground | −0.3 V to +6.5 V |
| VREF to Ground | −0.3 V to +6.5 V |
| FB1, FB2, FB3, FB4 to Ground [1] | −0.3 V to +6.5 V |
| COMP1, COMP2, COMP3, COMP4 to Ground | −0.3 V to +6.5 V |
| VSET1, VSET2, VSET3, VSET4 to Ground | −0.3 V to +6.5 V |
| Storage Temperate Range | −65°C to +150°C |
| Operational Junction Temperature Range | −40°C to +125°C |

[1] The rating for the FB1, FB2, FB3, and FB4 pins applies to the adjustable output voltage models of the ADP5014.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

**Table 4. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| CP-40-10 | 40 | 11.1 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

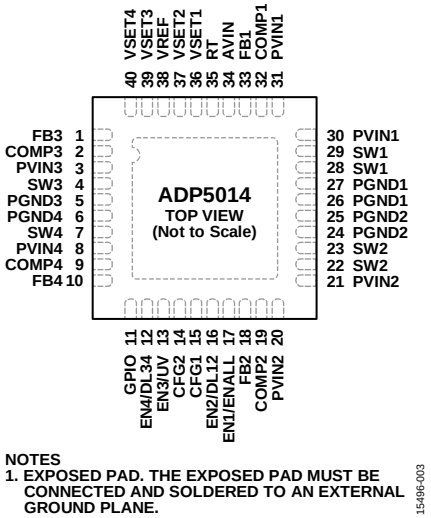



*Figure 3. Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | FB3 | Feedback Sensing Input for Channel 3. |
| 2 | COMP3 | Error Amplifier Output for Channel 3. Connect a resistor capacitor (RC) network from this pin to ground. |
| 3 | PVIN3 | Power Input for Channel 3. |
| 4 | SW3 | Switching Node Output for Channel 3. |
| 5 | PGND3 | Power Ground for Channel 3 |
| 6 | PGND4 | Power Ground for Channel 4. |
| 7 | SW4 | Switching Node Output for Channel 4. |
| 8 | PVIN4 | Power Input for Channel 4. |
| 9 | COMP4 | Error Amplifier Output for Channel 4. Connect an RC network from this pin to ground. |
| 10 | FB4 | Feedback Sensing Input for Channel 4. |
| 11 | GPIO | General-Purpose Input or Output Signal. This pin can be configured as power good, synchronization clock output (CLK-OUT) or undervoltage comparator output (UVO). |
| 12 | EN4/DL34 | Enable Input for Channel 4 in Manual Mode (EN4).<br>Delay Timer Setting for Channel 3 and Channel 4 in Sequence Mode (DL34). Connect one resistor from this pin to ground to program the start-up and shutdown sequence delay timer for Channel 3 and Channel 4. |
| 13 | EN3/UV | Enable Input for Channel 3 in Manual Mode (EN3).<br>Under Voltage Comparator Input in Sequence Mode (UV). |
| 14 | CFG2 | System Configuration Pin 1. Connect one resistor from this pin to ground to program sequence or manual mode, the delay timer, PSM or FPWM operation mode, and GPIO mapping for all channels. |
| 15 | CFG1 | System Configuration Pin 2. Connect one resistor from this pin to ground to program current limit, and the parallel output for all channels. |
| 16 | EN2/DL12 | Enable Input for Channel 2 in Manual Mode (EN2).<br>Delay Timer Setting for Channel 1 and Channel 2 in Sequence Mode (DL12). Connect one resistor from this pin to ground to program the start-up and shutdown sequence delay timer for Channel 1 and Channel 2. |
| 17 | EN1/ENALL | Enable Input for Channel 1 in Manual Mode (EN1).<br>Grouped Enable Input for All Channels in Sequence Mode (ENALL). |
| 18 | FB2 | Feedback Sensing Input for Channel 2. |
| 19 | COMP2 | Error Amplifier Output for Channel 2. Connect an RC network from this pin to ground. |
| 20, 21 | PVIN2 | Power Input for Channel 2. |
| 22, 23 | SW2 | Switching Node Output for Channel 2. |
| 24, 25 | PGND2 | Power Ground for Channel 2. |
| 26, 27 | PGND1 | Power Ground for Channel 1. |
| 28, 29 | SW1 | Switching Node Output for Channel 1. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 30, 31 | PVIN1 | Power Input for Channel 1. |
| 32 | COMP1 | Error Amplifier Output for Channel 1. Connect an RC network from this pin to ground. |
| 33 | FB1 | Feedback Sensing Input for Channel 1. |
| 34 | AVIN | Analog Power Input for the Internal Control Circuitry. Connect a bypass capacitor between this pin and ground. Connect a small (10 Ω) resistor between this pin and PVINx. |
| 35 | RT | Frequency Setting. Connect a resistor from RT to ground to program the switching frequency. |
| 36 | VSET1 | Channel 1 Reference Voltage Setting Input. |
| 37 | VSET2 | Channel 2 Reference Voltage Setting Input. |
| 38 | VREF | Internal Low Noise Voltage Reference Output. |
| 39 | VSET3 | Channel 3 Reference Voltage Setting Input. |
| 40 | VSET4 | Channel 4 Reference Voltage Setting Input. |
| | Exposed Pad | Analog Ground. The exposed pad must be connected and soldered to an external ground plane. |

# TYPICAL PERFORMANCE CHARACTERISTICS

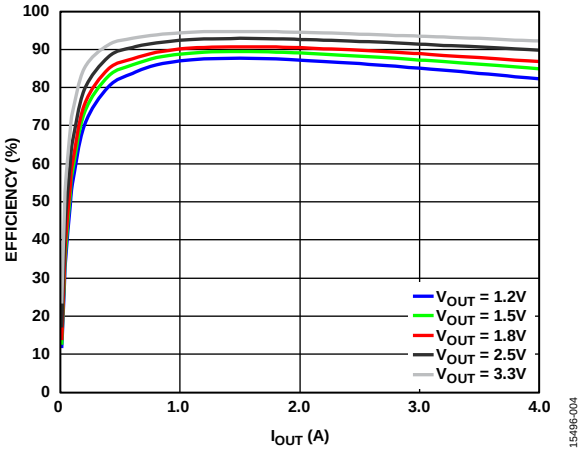



*Figure 4. Channel 1/Channel 2 Efficiency Curve, $V_{IN}$ = 5 V, $f_{SW}$ = 1.2 MHz, FPWM Mode*

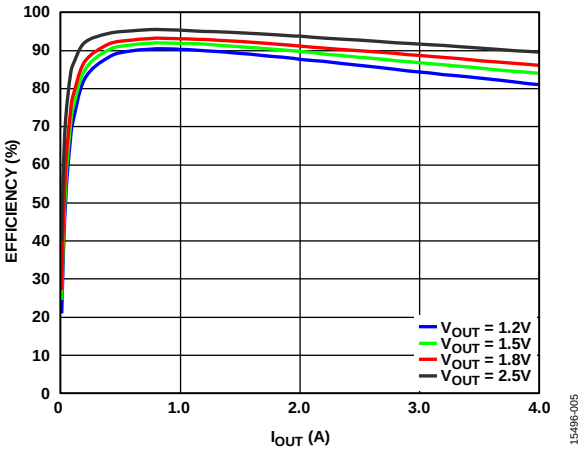



*Figure 5. Channel 1/Channel 2 Efficiency Curve, $V_{IN}$ = 3.3 V, $f_{SW}$ = 1.2 MHz, FPWM Mode*

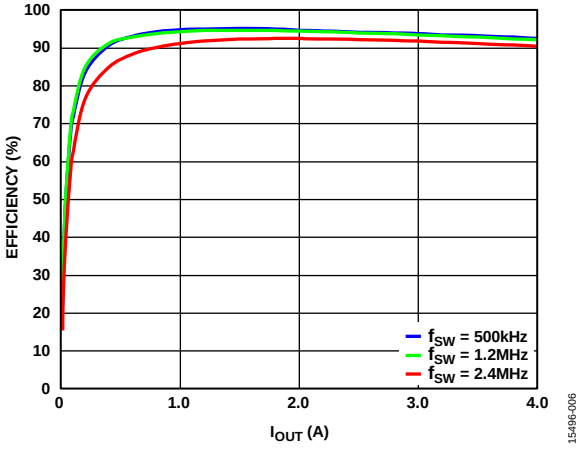



*Figure 6. Channel 1/Channel 2 Efficiency Curve, $V_{IN}$ = 5 V, $V_{OUT}$ = 3.3 V, FPWM Mode*

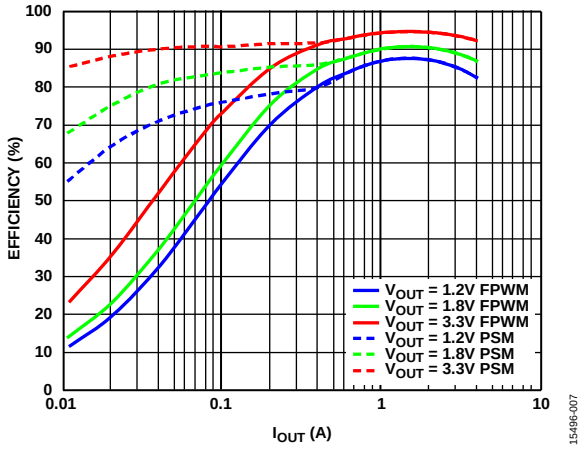



*Figure 7. Channel 1/Channel 2 Efficiency Curve, $V_{IN}$ = 5 V, $f_{SW}$ = 1.2 MHz, FPWM and Automatic PWM/PSM Modes*

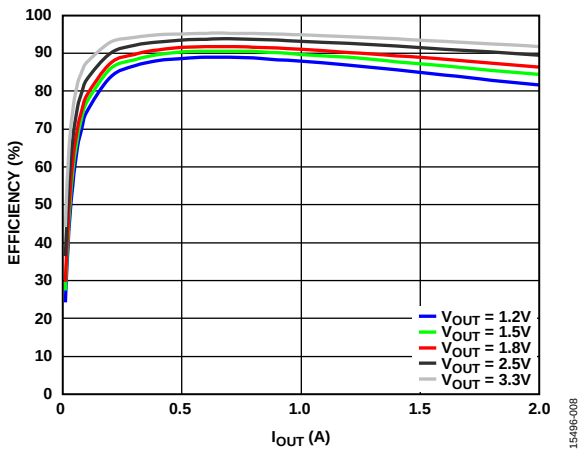



*Figure 8. Channel 3/Channel 4 Efficiency Curve, $V_{IN}$ = 5 V, $f_{SW}$ = 1.2 MHz, FPWM Mode*

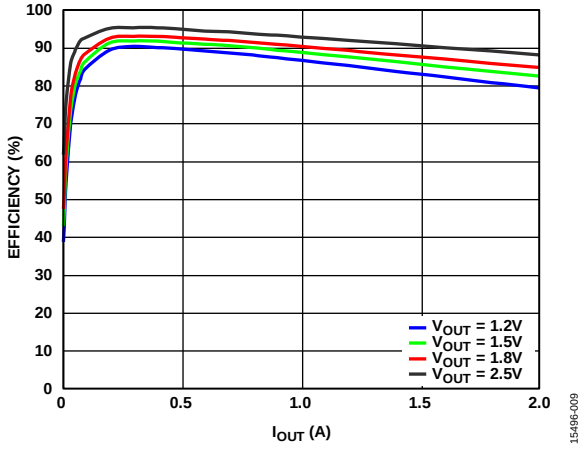



*Figure 9. Channel 3/Channel 4 Efficiency Curve, $V_{IN}$ = 3.3 V, $f_{SW}$ = 1.2 MHz, FPWM Mode*

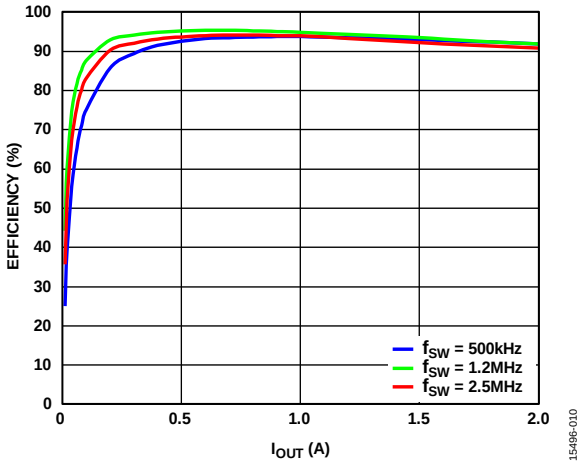



Figure 10. Channel 3/Channel 4 Efficiency Curve, $V_{IN}$ = 5 V, $V_{OUT}$ = 3.3 V, FPWM Mode

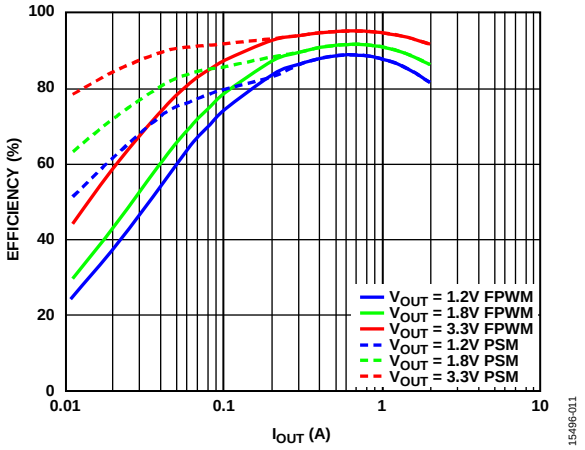



Figure 11. Channel 3/Channel 4 Efficiency Curve, $V_{IN}$ = 5 V, $f_{SW}$ = 1.2 MHz, FPWM and Automatic PWM/PSM Modes

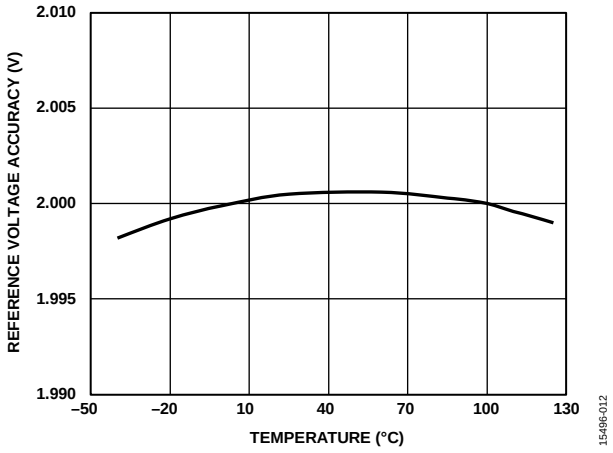



Figure 12. 2.0 V Reference Voltage Accuracy vs. Temperature

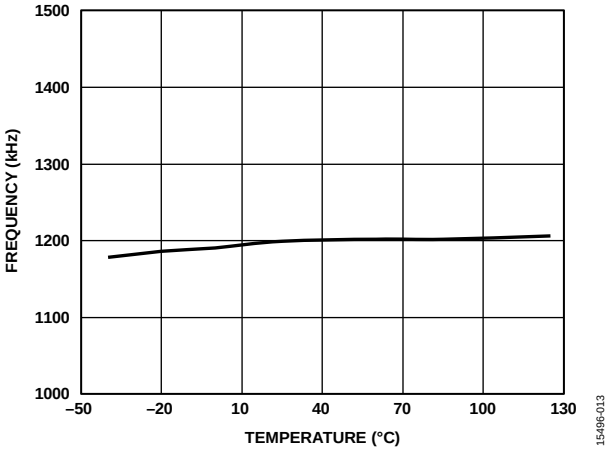



Figure 13. Frequency vs. Temperature, $V_{IN}$ = 5 V, $f_{SW}$ = 1.2 MHz

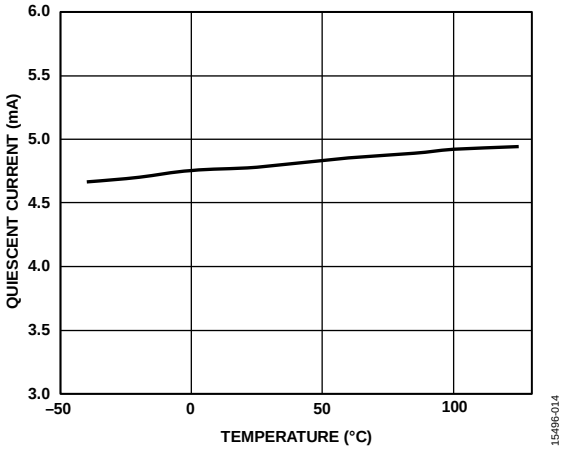



Figure 14. Quiescent Current vs. Temperature (Includes PVIN1, PVIN2, PVIN3, and PVIN4)

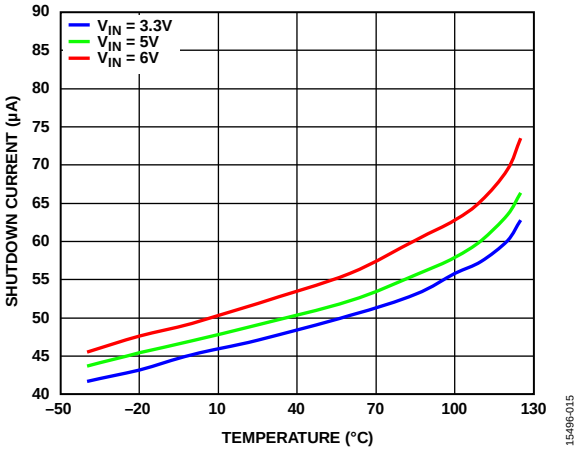



Figure 15. Shutdown Current vs. Temperature (EN1/ENALL, EN2/DL12, EN3/UV, and EN4/DL34 Low)

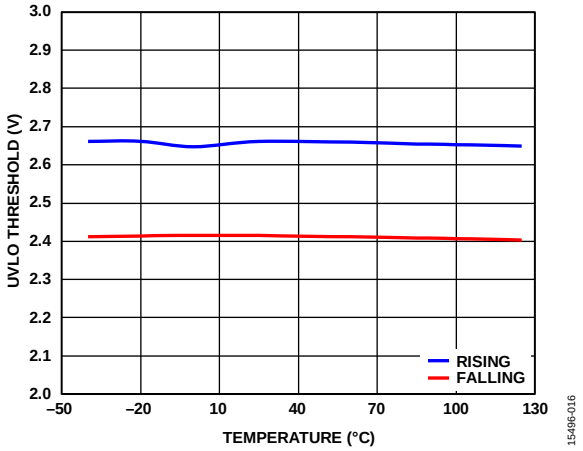



Figure 16. UVLO Threshold vs. Temperature

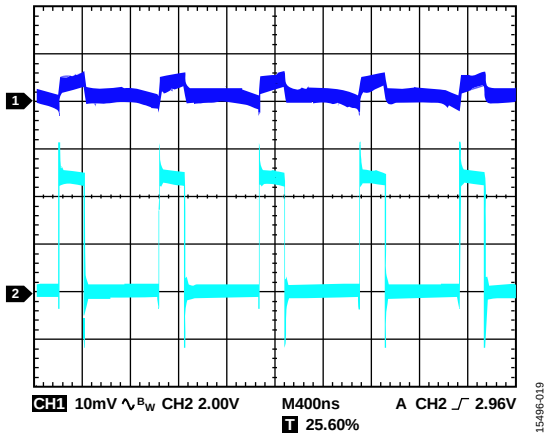



Figure 19. Steady State Waveform at Heavy Load, $V_{IN}$ = 5 V, $V_{OUT}$ = 1.2 V, $I_{OUT}$ = 3 A, $f_{SW}$ = 1.2 MHz, L = 0.8 µH, $C_{OUT}$ = 47 µF × 2, FPWM Mode, Channel 1 = $V_{OUTX}$, Channel 2 = $SW_X$

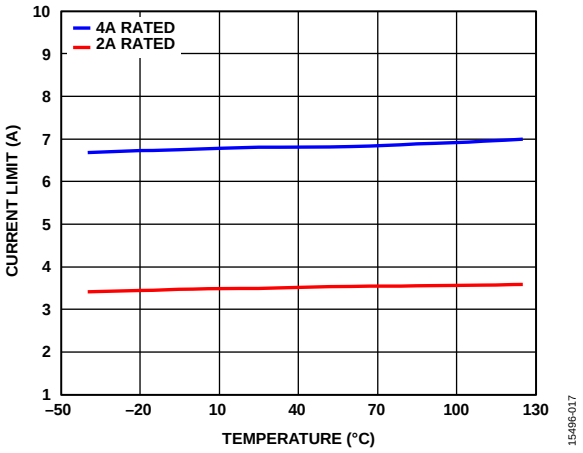



Figure 17. Channel 1/Channel 2 Current Limit vs. Temperature

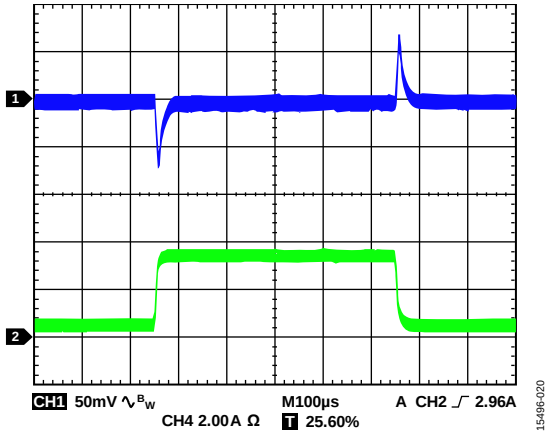



Figure 20. Channel 1/Channel 2 Load Transient, 0.5 A to 3.5 A, $V_{IN}$ = 5 V, $V_{OUT}$ = 1.2 V, $f_{SW}$ = 1.2 MHz, L = 0.8 µH, $C_{OUT}$ = 47 µF × 2, Channel 1 = $V_{OUTX}$, Channel 2 = $I_{OUTX}$

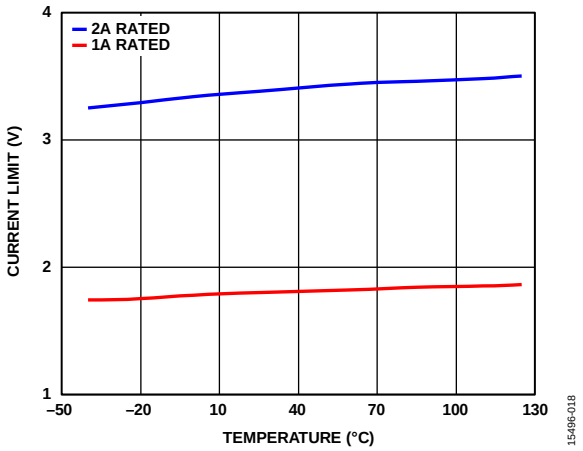



Figure 18. Channel 3/Channel 4 Current Limit vs. Temperature

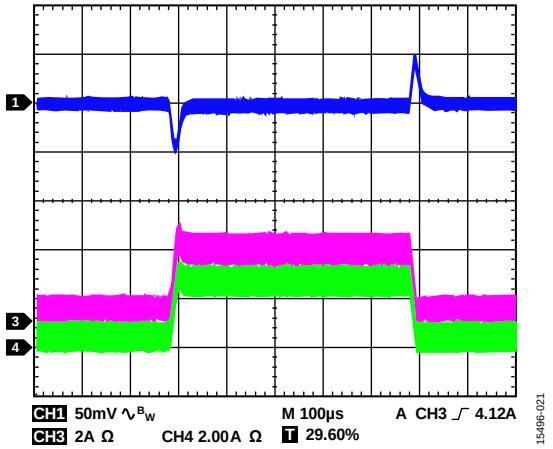



Figure 21. Load Transient, Channel 1/Channel 2 Parallel Output, 1 A to 6 A, $V_{IN}$ = 5 V, $V_{OUT}$ = 1.2 V, $f_{SW}$ = 1.2 MHz, L = 0.8 µH, $C_{OUT}$ = 47 µF × 4, Channel 1 = $V_{OUT}$, Channel 3 = $I_{L1}$, Channel 4 = $I_{L2}$

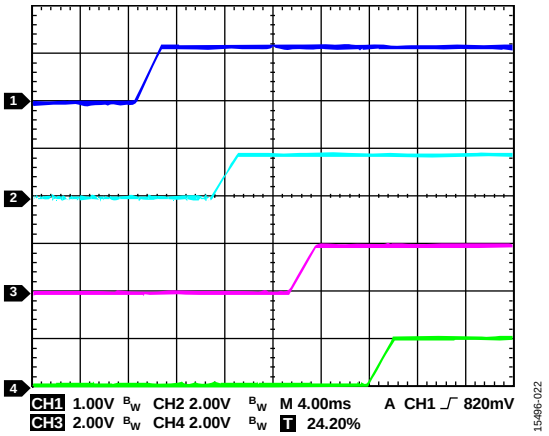



Figure 22. Startup for All Channels Under Sequence Enable Mode, Channel 1 = $V_{OUT1}$, Channel 2 = $V_{OUT2}$, Channel 3 = $V_{OUT3}$, Channel 4 = $V_{OUT4}$

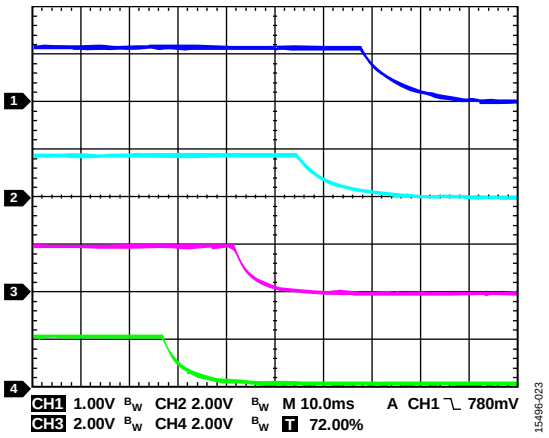



Figure 23. Shutdown for All Channels Under Sequence Enable Mode, Channel 1 = $V_{OUT1}$, Channel 2 = $V_{OUT2}$, Channel 3 = $V_{OUT3}$, Channel 4 = $V_{OUT4}$

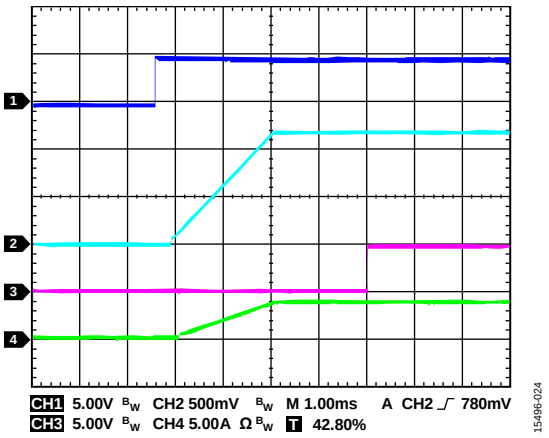



Figure 24. Channel 1 Startup with Full Load, $V_{IN}$ = 5 V, $V_{OUT}$ = 1.2 V, Channel 1 = EN1/ENALL, Channel 2 = $V_{OUT1}$, Channel 3 = PWRGD, Channel 4 = $I_{OUT1}$

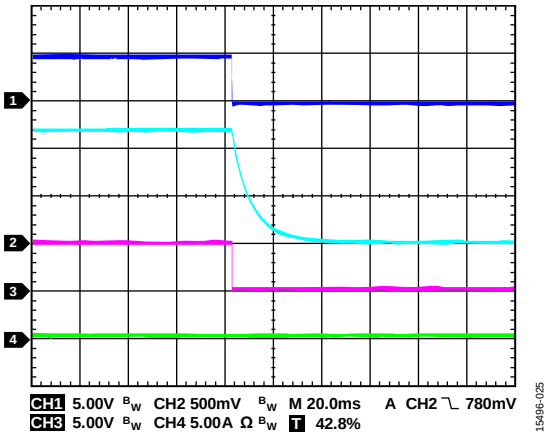



Figure 25. Channel 1 Shutdown with Active Output Discharge, $V_{IN}$ = 5 V, $V_{OUT}$ = 1.2 V, $f_{SW}$ = 1.2 MHz, L = 0.8 µH, $C_{OUT}$ = 47 µF × 2, Channel 1 = EN1/ENALL, Channel 2 = $V_{OUT1}$, Channel 3 = PWRGD, Channel 4 = $I_{OUT1}$

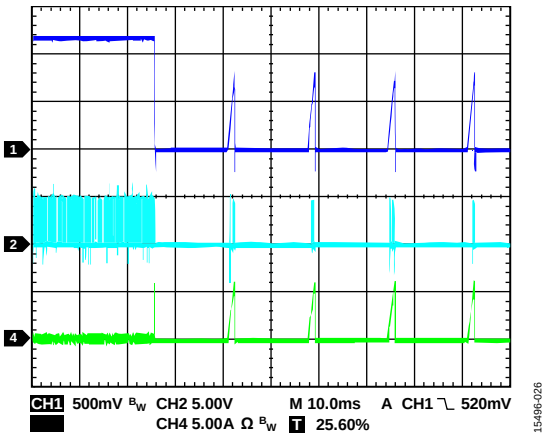



Figure 26. Short-Circuit Protection Entry, $V_{IN}$ = 5 V, $V_{OUT}$ = 1.2 V, $f_{SW}$ = 1.2 MHz, L = 0.8 µH, $C_{OUT}$ = 47 µF × 2, Channel 1 = $V_{OUTX}$, Channel 2 = $SW_X$, Channel 4 = $I_{LX}$

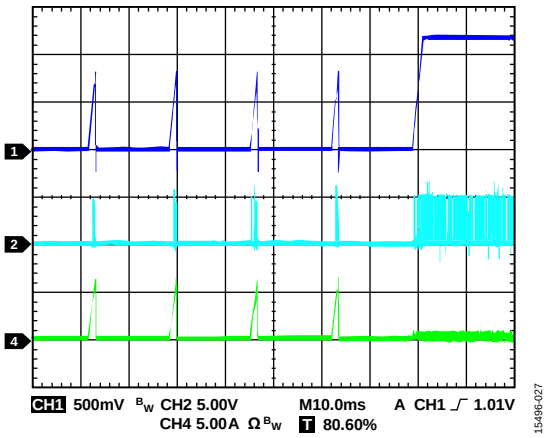



Figure 27. Short-Circuit Protection Recovery, $V_{IN}$ = 5 V, $V_{OUT}$ = 1.2 V, $f_{SW}$ = 1.2 MHz, L = 0.8 µH, $C_{OUT}$ = 47 µF × 2, Channel 1 = $V_{OUTX}$, Channel 2 = $SW_X$, Channel 4 = $I_{LX}$

# THEORY OF OPERATION

The ADP5014 is a power management unit that combines four high performance, low noise buck regulators in a 40-lead LFCSP package.

## BUCK REGULATOR OPERATIONAL MODES

### *PWM Mode*

In PWM mode, the buck regulators in the ADP5014 operate at a fixed frequency; this frequency is set by an internal oscillator that is programmed by the RT pin. At the start of each oscillator cycle, the high-side MOSFET switch turns on and sends a positive voltage across the inductor. The inductor current increases until the current sense signal exceeds the peak inductor current threshold that turns off the high-side MOSFET switch. This threshold is set by the error amplifier output. During the high-side MOSFET off time, the inductor current decreases through the low-side MOSFET switch until the next oscillator clock pulse starts a new cycle. The buck regulators in the ADP5014 regulate the output voltage by adjusting the peak inductor current threshold.

### *PSM Mode*

To achieve higher efficiency, the buck regulators in the ADP5014 smoothly transition to variable frequency PSM mode operation when the output load falls below the PSM current threshold. When the output voltage falls below regulation, the buck regulator enters PWM mode for a few oscillator cycles until the voltage increases to within regulation. During the idle time between bursts, the MOSFET switch turns off, and the output capacitor supplies all the output current.

The PSM mode comparator monitors the internal compensation node, which represents the peak inductor current information. The average PSM mode current threshold depends on the input voltage ($V_{IN}$), the output voltage ($V_{OUT}$), the inductor, and the output capacitor. Because the output voltage occasionally falls below regulation and then recovers, the output voltage ripple in PSM mode is larger than the ripple in the forced PWM mode of operation under light load conditions.

### *FPWM and Automatic PWM/PSM Modes*

The buck regulators can be configured to always operate in FPWM mode using the CFG2 configuration pin. In forced PWM mode, the regulator continues to operate at a fixed frequency even when the output current is below the PWM/PSM threshold. In PWM mode, the efficiency is lower compared to PSM mode under light load conditions. The low-side MOSFET remains on when the inductor current falls to less than 0 A, causing the ADP5014 to enter continuous conduction mode (CCM).

The buck regulators can be configured to operate in automatic PWM or PSM mode using the CFG2 configuration pin. In automatic PWM/PSM mode, the buck regulators operate in either PWM mode or PSM mode, depending on the output current. When the average output current falls below the PWM/PSM threshold, the buck regulator enters PSM mode operation; in PSM mode, the regulator operates with a reduced switching frequency to maintain high efficiency. The low-side MOSFET turns off when the output current reaches 0 A, causing the regulator to operate in discontinuous mode (DCM).

Use the CFG2 pin to configure the operational mode of all four buck regulators to operate in PWM mode or automatic PWM/PSM mode.

## LOW NOISE ARCHITECTURE

Traditional dc-to-dc or linear regulator output noise is typically proportional to the output voltage setting. The ADP5014 optimizes many analog blocks to achieve lower output noise at low frequency range. The unity-gain voltage reference structure also makes its output noise independent from the output voltage setting when $V_{OUT}$ setting is less than $V_{REF}$ voltage.

The low noise buck regulator enables the device to power up noise sensitive signal chain products directly with excellent output noise performance, ~25 μV rms from 10 Hz to 100 kHz, which is similar or even better than traditional low dropout regulators (LDOs).

The additional LC filter is still required because the fundamental switching output ripple and its harmonic affects signal chain performance and likely generates unexpected spurs. This additional LC filter is typically relatively small due to the high switching frequency operation of the buck regulator in the ADP5014.

## INTERNAL REFERENCE (VREF)

The ADP5014 provides an accurate, low noise, 2.0 V reference voltage. One 0.47 μF ceramic capacitor must be connected between VREF and ground. A larger value of capacitance provides better noise suppression.

The VREF reference circuitry is mainly designed for internal use and has very limited output load capacity (<1 mA); therefore, check the load capability requirements if VREF is used for other purposes.

## ADJUSTABLE OUTPUT VOLTAGE

The ADP5014 provides adjustable output voltage settings via the external resistor divider. To minimize output noise and maintain the loop unity-gain, the device provides the reference input path to the error amplifier input with the integrated low-frequency filter for each channel. Use an external resistor divider to set the desired output voltage. Figure 28 shows the adjustable output voltage diagram.

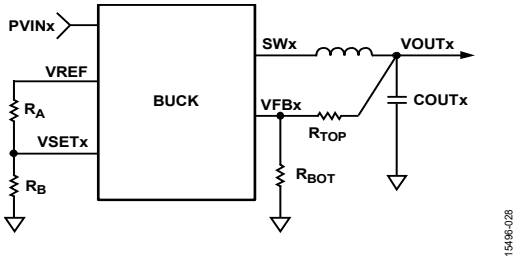



*Figure 28. Adjustable Output Voltage Configuration*

## FUNCTION CONFIGURATIONS (CFG1 AND CFG2)

The ADP5014 include CFG1 and CFG2 pins to decode the function configurations for all channels. The CFG1 pin has a logic status of 8 that is decoded by connecting one resistor to ground, whereas the CFG2 pin has a logic status of 16, decoded by connecting one resistor to ground. This decoder circuitry only works in the initiation stage of the ADP5014; therefore, the configurations cannot be changed in operation. Typically, the chip initiation takes less than 1 ms before the enabled regulator starts switching.

The CFG1 pin can be used to program the load output capability and parallel operation for all channels. Table 6 provides the values of the resistors needed to set different functionality in the CFG1 pin.

**Table 6. Configuration by the CFG1 Pin**

| | Output Capability | | | |
|---|---|---|---|---|
| $R_{CFG1}$ (kΩ) | Channel 1 | Channel 2 | Channel3 | Channel 4 |
| 0 | 4 A | 4 A | 2 A | 2 A |
| 10 | 4 A | 2 A | 2 A | 2 A |
| 12.1 | 4 A | 2 A | 1 A | 1 A |
| 14.7 | 2 A | 2 A | 2 A | 2 A |
| 17.8 | 2 A | 2 A | 1 A | 1 A |
| 21.5 | Parallel 8A | Parallel 8 A | 2 A | 2 A |
| 26.1 | 4 A | 4 A | Parallel 4 A | Parallel 4 A |
| 31.6 | Parallel 8 A | Parallel 8 A | Parallel 4 A | Parallel 4 A |

The CFG2 pin can be used to program the operation mode (FPWM or PWM/PSM mode), the enable mode (manual mode or sequence mode), the timer (×1 or ×8), and GPIO functionalities (PWRGD, SYNC-IN, CLK-OUT, UVO) for all channels. Table 7 provides the values of the resistors needed to set different functionality in the CFG2 pin.

The $R_{CFG1}$ and $R_{CFG2}$ resistors must have ±1% tolerance to ensure the correct decoding result.

**Table 7. Configuration by the CFG2 Pin**

| $R_{CFG2}$ (kΩ) | Enable Mode | Timer | Operation Mode | GPIO |
|---|---|---|---|---|
| 0 | Manual | ×1 | FPWM | PWRGD |
| 10 | Manual | ×1 | FPWM | SYNC-IN |
| 12.1 | Manual | ×1 | FPWM | CLK-OUT |
| 14.7 | Manual | ×1 | PSM | PWRGD |
| Float | Manual | ×8 | FPWM | PWRGD |
| 17.8 | Manual | ×8 | FPWM | SYNC-IN |
| 21.5 | Manual | ×8 | FPWM | CLK-OUT |
| 26.1 | Manual | ×8 | PSM | PWRGD |
| 31.6 | Sequence | ×1 | FPWM | UVO |
| 38.3 | Sequence | ×1 | FPWM | SYNC-IN |
| 46.4 | Sequence | ×1 | FPWM | CLK-OUT |
| 56.2 | Sequence | ×1 | PSM | UVO |
| 68.1 | Sequence | ×8 | FPWM | UVO |
| 82.5 | Sequence | ×8 | FPWM | SYNC-IN |
| 100 | Sequence | ×8 | FPWM | CLK-OUT |
| 121 | Sequence | ×8 | PSM | UVO |

## PARALLEL OPERATION

The ADP5014 supports 2-phase parallel operation of Channel 1 and Channel 2 to provide a single output with up to 8 A of current, and two-phase parallel operation of Channel 3 and Channel 4 to provide a single output with up to 4 A of current. To configure a 2-phase single output in parallel operation, perform the following steps (see Figure 29). Use the CFG1 pin to select parallel operation as specified in Table 7.

- Leave the COMP2 pin (or COMP4 pin) open.
- Use the VSET1 and FB1 pin (or VSET3 and FB3 pin) to set the output voltage.
- Connect the FB2 and VSET2 pin (or FB4 pin and VSET4) to ground (FB2 is ignored). Connect the EN2/DL12 pin (or EN4/DL34 pin) to ground in manual enable mode (EN2 is ignored). Note that the EN2/DL12 pin is for the delay timer configuration in sequence enable mode.

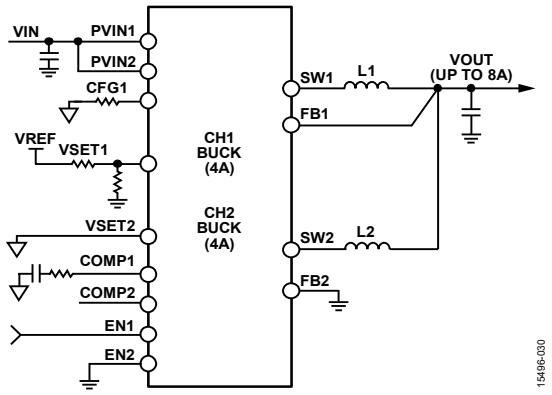



*Figure 29. Parallel Operation for Channel 1 and Channel 2*

The following considerations apply when two channels are operating in the parallel configuration:

- The input voltages for both channels are the same.
- Both channels are operating in forced PWM mode.
- Do not support sequence mode.

The current balance in parallel configuration is well regulated by the internal control loop. Figure 30 shows the typical current balance matching in the parallel output configuration.

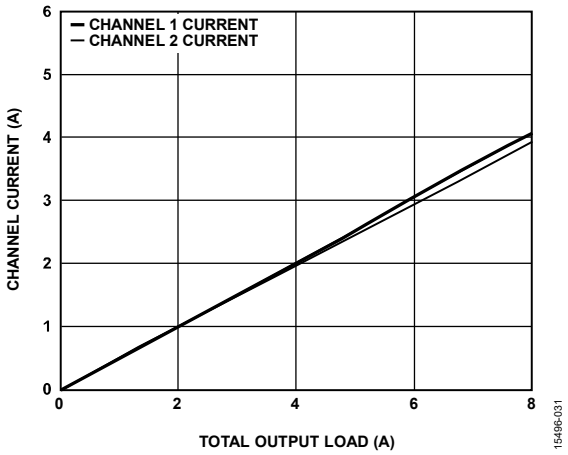



*Figure 30. Current Balance in Parallel Output Configuration, $V_{IN}$ = 5 V, $V_{OUT}$ = 1.2 V, $f_{SW}$ = 1.2 MHz, FPWM Mode*

## MANUAL/SEQUENCE MODE

The ADP5014 features two enable modes using the CFG2 pin configuration. The manual mode has individual precision enable pins to enable each regulator manually. Alternatively, the sequence mode has one grouped precision enable signal with a programmable power-up and power-down delay timer on each rail.

The enable pin (EN1 to EN4) functionality is different in manual mode and sequence mode. Note that throughout this data sheet, multifunction pins, such as EN1/ENALL, are referred to by either the entire pin name or by a single function of the pin, for example, EN1, when only that format is relevant. Figure 31 and Table 8 show the pin mapping in different enable modes.

If some channels are unused, pull down the corresponding PVINx and ENx pin to ground and leave the SWx, COMPx, VSETx, and FBx pins floating.

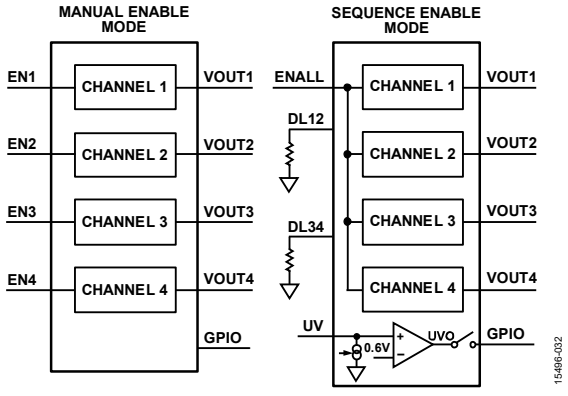



*Figure 31. Pin Configuration in Different Enable Modes*

**Table 8. Pin Functionality in Different Enable Modes**

| Pin Name | Manual Enable Mode | Sequence Enable Mode |
|---|---|---|
| EN1/ENALL (Pin 17) | EN1—enable pin for Channel 1 | ENALL—grouped enable pin for all four channels |
| EN2/DL12 (Pin 16) | EN2—enable pin for Channel 2 | DL12—delay timer setting for Channel 1 and Channel 2 |
| EN3/UV (Pin 13) | EN3—enable pin for Channel 3 | UV—undervoltage comparator input |
| EN4/DL34 (Pin 12) | EN4—enable pin for Channel 4 | DL34—delay timer setting for Channel 3 and Channel 4 |

### Manual Mode (Precision Enable)

In manual mode, the ADP5014 has an individual precision enable pin for each regulator. The enable control pin (ENx) features a precision enable circuit with a 0.6 V reference voltage. When the voltage at the ENx pin is greater than 0.6 V (typical), the regulator is enabled. When the ENx pin voltage falls below 0.57 V (typical), the regulator is disabled. To force the regulator to automatically start up when input power is applied, connect the enable pin to the input.

The precision enable pin has an internal pull-down current source (4 µA) that provides a default turn off when the enable pin is left open. When the enable pin exceeds 0.6 V (typical), the regulator is enabled and the internal pull-down current source at the enable pin decreases to 1 µA. The decrease in the current source allows the ratio of the external resistor divider to program the UVLO threshold to monitor either the input voltage or the output voltage while using the absolute value of external resistor divider to program the hysteresis window. Figure 32 shows the precision enable diagram.

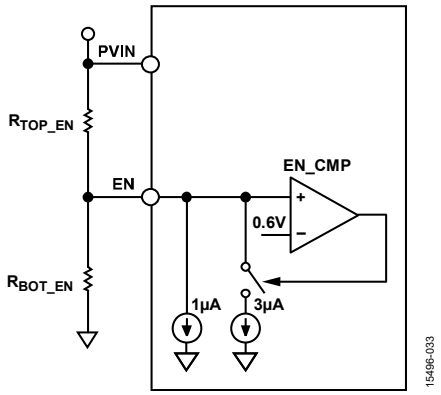



*Figure 32. Precision Enable Diagram for One Channel*

### Sequence Mode

In sequence mode, all channels in the ADP5014 turn on and off under the control of the internal sequencer, which is triggered by the ENALL pin. The DL12 and DL34 pins set the predefined delay timer.

The ENALL pin features precision enable circuitry with a 0.6 V turn on threshold and internal pull-down current source. When the ENALL pin goes above the 0.6 V precision threshold, all channels controlled by the sequencer begin a soft start after the delay time specified by the DL12 and DL34 pin configuration. Similarly, when the ENALL pin falls below 0.57 V precision threshold, the channels turns off after the delay time specified by DL12 and DL34 pin configurations.

Figure 33 shows the logical states of each channel and does not show soft start and discharge ramps. Although the output discharge switch helps to discharge the output capacitor quickly, the discharge ramps on the output of each channel are still decided by many different factors, including the output capacitance, system load, and the ramps of input supply.

DL12 configures the delay timer for Channel 1 and Channel 2 by connecting one resistor to ground. Similarly, DL34 configures the delay timer for Channel 3 and Channel 4 (see Table 9). In parallel operation, the slave channel (Channel 2 or Channel 4) always follows up with the delay timer configuration of the master channel; therefore, Channel 2 follows Channel 1, while Channel 4 follows Channel 3. The delay timer decoder circuitry only works in the initiation stage of the ADP5014; therefore, the delay timer does not change in operation.

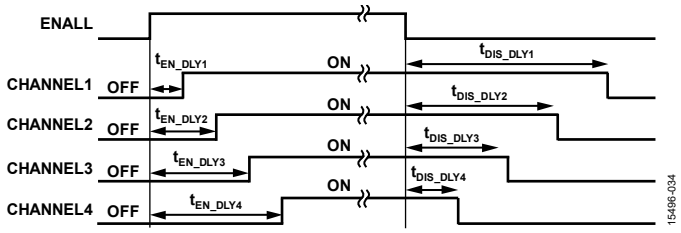



*Figure 33. Power-Up/Power-Down in Sequence Enable Mode*

**Table 9. Setting Sequence Timer in the DL12 and DL34 Pins**

| $R_{DL12}$ (or $R_{DL34}$) (kΩ) | Channel 1 Sequence (or Channel 3) | Channel 2 Sequence (or Channel 4) |
|---|---|---|
| 10 | First order | First order |
| 0 | First order | Second order |
| 12.1 | First order | Third order |
| 14.7 | First order | Fourth order |
| 17.8 | Second order | First order |
| 21.5 | Second order | Second order |
| 26.1 | Second order | Third order |
| 31.6 | Second order | Fourth order |
| 38.3 | Third order | First order |
| 46.4 | Third order | Second order |
| 56.2 | Third order | Third order |
| Float | Third order | Fourth order |
| 68.1 | Fourth order | First order |
| 82.5 | Fourth order | Second order |
| 100 | Fourth order | Third order |
| 121 | Fourth order | Fourth order |

Note that the $R_{DL12}$ and $R_{DL34}$ resistors must have ±1 % tolerance to ensure the correct decoding result.

The power-up and power-down delay timer for all channels is designed in an opposite manner to meet typical system sequence requirements, as described below:

- First order sequence means the channel is configured as the first to be powered up, and is shut down last.
- Second order sequence means the channel is configured as the second to be powered up and is shut down third.
- Third order sequence means the channel is configured as the third to be powered up and is shut down second.
- Fourth order sequence means the channel is configured as the fourth to be powered up and is shut down first.

If a longer sequence timer is required, the delay time for all channels can be increased by 8 times (×8 option) using the CFG2 pin. Table 10 shows the power-up and power-down timer configurations.

In sequence enable mode, the device performs the following actions in fault conditions:

- During individual fault conditions, such as overcurrent hiccup, OVP, or PVINx, UVLO shuts down and powers up the corresponding channel immediately without the sequence delay.
- TSD fault shuts down all channels immediately without the sequence delay, but occurs after the defined power-up sequence for the recovery.
- An AVIN UVLO fault shuts down all channels immediately without any sequence delay, but occurs after the defined power-up sequence for the recovery after the device reinitiation.

**Table 10. Power-Up and Power-Down Timer**

| Sequence Order | Power-Up Delay Timer ($t_{EN\_DLYx}$) | Power-Down Delay Timer ($t_{DIS\_DLYx}$) |
|---|---|---|
| First Order | 0 ms | 36 ms (288 ms at ×8 option) |
| Second Order | 6 ms (48 ms at ×8 option) | 24 ms (192 ms at ×8 option) |
| Third Order | 12 ms (96 ms at ×8 option) | 12 ms (96 ms at ×8 option) |
| Fourth Order | 18 ms (144 ms at ×8 option) | 0 ms |

## GENERAL PURPOSE INPUT/OUTPUT (GPIO)

The ADP5014 includes one GPIO pin which can be configured for different functionalities, such as PWRGD, synchronization clock input (SYNC-IN), CLK-OUT, or UVO.

The PWRGD and UVO output functionalities have the open-drain output after the initiation.

The CLK-OUT output functionality features a push/pull output, enabling it to drive other regulators after initiation.

## OSCILLATOR

The switching frequency ($f_{SW}$) of the ADP5014 can be set to a value from 500 kHz to 2.5 MHz by connecting a resistor from the RT pin to ground. Calculate the value of the RT resistor ($R_{RT}$) as follows:

$$R_{RT}\,(\text{k}\Omega) = 100{,}000/f_{SW}\,(\text{kHz})$$

Figure 34 shows the typical relationship between $f_{SW}$ and the RT resistor. The adjustable frequency allows users to make decisions based on the trade-off between efficiency and the size of the solution.

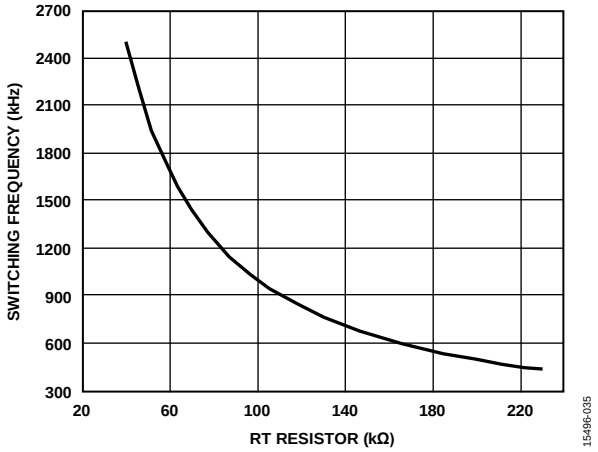



*Figure 34. Switching Frequency vs. RT Resistor*

### *Phase Shift*

By default, the phase shift between Channel 1 and Channel 2 and between Channel 3 and Channel 4 is 180° (see Figure 35). This value provides the benefits of out of phase operation by reducing the input ripple current and lowering the grounding noise.

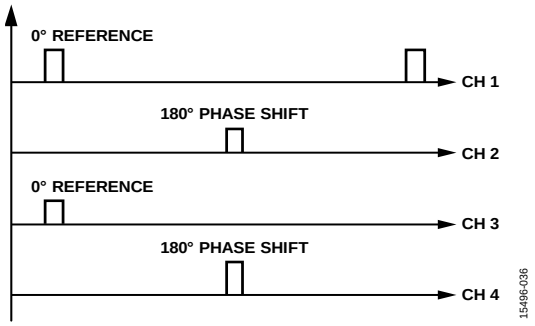



*Figure 35. Phase Shift Diagram, Four Buck Regulators*

## SYNCHRONIZATION INPUT/OUTPUT

The GPIO pin can be configured as the synchronization clock input by using the CFG2 pin (see Table 7), and the switching frequency of the ADP5014 can be synchronized to an external clock with a frequency range from 500 kHz to 2.5 MHz. The ADP5014 automatically detects the presence of an external clock applied to the GPIO pin, and the switching frequency transitions smoothly to the frequency of the external clock. When the external clock signal stops, the device automatically switches back to the internal clock and continues to operate.

The internal switching frequency set by the RT pin must be programmed to a value that is close to the external clock value for successful synchronization; the suggested frequency difference is less than ±15% in typical applications.

The GPIO pin can be configured as a push/pull synchronization clock output by CFG2 (refer to Table 7). A positive clock pulse with a 50% duty cycle is generated at the GPIO pin with a frequency equal to the internal switching frequency set by the RT pin.

Figure 36 shows two ADP5014 devices configured for frequency synchronization mode: one ADP5014 device is configured as the clock output to synchronize another ADP5014 device.

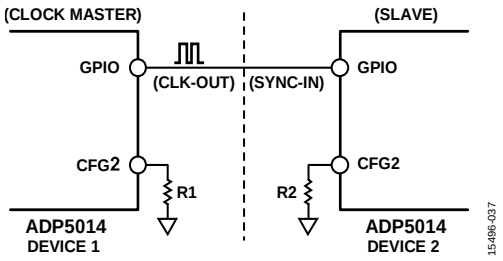



*Figure 36. Two ADP5014 Devices Configured for Synchronization Mode*

In the configuration shown in Figure 36, the phase shift between Channel 1 of the first ADP5014 device and Channel 1 of the second ADP5014 device is 0˚.

## POWER-GOOD FUNCTION

The ADP5014 GPIO pin can be configured as an open-drain power-good output (PWRGD pin) that becomes active high when the selected buck regulators are operating normally.

A high status in the PWRGD pin indicates that the regulated output voltage of the buck regulator is above 90% (typical) of its nominal output. When the regulated output voltage of the buck regulator falls below 87% (typical) of its nominal output for a delay time greater than approximately 50 µs, the status of the PWRGD pin is set to low.

The output of the PWRGD pin is the logical AND of the internal PWRGD signals on an individual channel. An internal PWRGD signal on an individual channel must be high for a validation time of 2 ms (typical) timer before the PWRGD pin goes high. This validation timer can be increased by 8 times (×8 option) using the CFG2 pin configuration; if one internal PWRGD fails, the PWRGD pin goes low with no delay.

## UV COMPARATOR (SEQUENCE MODE ONLY)

In sequence mode, the EN3/UV pin is used as the UVO input (UV pin), while the ADP5014 GPIO pin can be configured as an open-drain UVO via CFG2 pin configuration. The UV comparator is not related to the channel enabling and is only used for monitoring purposes. For example, it can be used to monitor any output voltage to create a power-good signal in sequence mode.

Similar to the precision enable functionality, this UVO features the same precise 0.6 V reference voltage with the 1 µA or 4 µA pull-down hysteresis current. Using the ratio of external resistor divider to program the UVLO threshold allows monitoring either input voltage or output voltage while using the absolute value of the external resistor divider to program the hysteresis window. The UV pin is connected to the input supply if it is not intended for use. Figure 37 shows the UVO diagram.

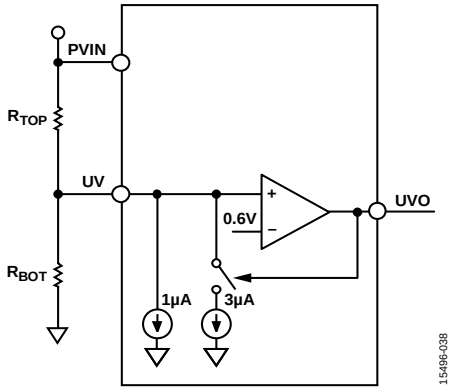



*Figure 37. Undervoltage Comparator Diagram (in Sequence Mode Only)*

## SOFT START

The buck regulators in the ADP5014 include soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current. The soft start time for all channels is typically fixed at 2 ms. The soft start time for all channels can be increased by eight times using the CFG2 pin configuration.

## STARTUP WITH PRECHARGED OUTPUT

The buck regulators in the ADP5014 include a precharged startup feature to protect the low-side FETs from damage during startup. If the output voltage is precharged before the regulator is turned on, the regulator prevents reverse inductor current, which discharges the output capacitor, until the internal soft start reference voltage exceeds the precharged voltage on a feedback (FBx) pin.

## CURRENT-LIMIT PROTECTION

The buck regulators in the ADP5014 include peak current-limit protection circuitry to limit the amount of positive current flowing through the high-side MOSFET switch. The peak current limit on the power switch limits the amount of current that can flow from the input to the output. The programmable current-limit threshold feature allows the use of small size inductors for low current applications.

To configure different output load capability, connect a resistor from the CFG1 pin to ground according to Table 6 which lists different output current capability settings for all channels.

The buck regulators in the ADP5014 include negative current-limit protection circuitry to limit certain amounts of negative current flowing through the low-side MOSFET switch.

## FREQUENCY FOLD BACK

The buck regulators in the ADP5014 include frequency fold back to prevent output current runaway when a hard short occurs on the output. Frequency fold back is implemented as follows:

- If the voltage at the FBx pin falls below half of the target output voltage, the switching frequency is reduced by half.
- If the voltage at the FBx pin falls again to below one-fourth of the target output voltage, the switching frequency is reduced by half of its current value again, equaling one-fourth of $f_{SW}$.

The reduced switching frequency allows more time for the inductor current to decrease, but also increases the ripple current during peak current regulation. The reduced switching frequency results in a reduction in average current and prevents output current runaway.

## SHORT-CIRCUIT PROTECTION (SCP)

The buck regulators in the ADP5014 include a hiccup mode for OCP. When the peak inductor current reaches the current-limit threshold, the high-side MOSFET turns off and the low-side MOSFET turns on until the next cycle.

When hiccup mode is active, the overcurrent fault counter is incremented. If the overcurrent fault counter reaches 15 and overflows (indicating a short-circuit condition), both the high-side and low-side MOSFETs are turned off. The buck regulator remains in hiccup mode for a period equal to seven soft start cycles and then attempts to restart from soft start. If the short-circuit fault has cleared, the regulator resumes normal operation; otherwise, it reenters hiccup mode after the soft start.

Hiccup detection is masked during the initial soft start cycle to enable startup of the buck regulator under heavy load conditions. Careful design and proper component selection are required to ensure the buck regulator recovers from hiccup mode under heavy loads.

In parallel operation, the overcurrent protection in either channel triggers both master and slave channels entering and exiting the hiccup protection together.

## OVERVOLTAGE PROTECTION

The ADP5014 includes an overvoltage protection feature to protect the regulator against an output short to a higher voltage supply, or when a strong load disconnect transient occurs. If the feedback voltage increases to 1.15 × VSETx, the internal high-side and low-side MOSFETs are turned off until the voltage at the FBx pin decreases to 1.1 × VSETx At that time, the ADP5014 resumes normal operation.

## UNDERVOLTAGE LOCKOUT

UVLO circuitry monitors the input voltage level of each buck regulator, including the analog input pin in the ADP5014. If any input voltage (PVINx pin) falls below 2.40 V (typical), the corresponding channel is turned off. After the input voltage rises above 2.65 V (typical), the soft start period is initiated, and the corresponding channel is enabled when the ENx pin is high.

A UVLO condition on the AVIN pin has a higher priority than a UVLO condition on individual channels, which means the AVIN pin supply must be available before individual channels can be operated.

The ADP5014 supports separate input voltages for buck regulators. This means that the input voltages for each individual buck regulator can be connected to different supply voltages, as long as its input voltage (PVINx pin) and its AVIN pin voltage are above its UVLO threshold.

## ACTIVE OUTPUT DISCHARGE SWITCH

Each buck regulator in the ADP5014 integrates a discharge switch from the switching node to ground. This switch is turned on when its associated regulator is disabled, which helps discharge the output capacitor quickly. The typical value of the discharge switch is 85 Ω for Channel 1 to Channel 4.

## THERMAL SHUTDOWN

If the ADP5014 junction temperature exceeds 150°C, the thermal shutdown circuit turns off the IC except for the internal linear regulator. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 15°C hysteresis is included so that the ADP5014 does not return to operation after thermal shutdown until the on-chip temperature falls below 135°C. When the device exits thermal shutdown, a soft start is initiated for each enabled channel.

# APPLICATIONS INFORMATION

## ADIsimPOWER DESIGN TOOL

The ADP5014 is supported by the ADIsimPower™ design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic and bill of materials and to calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and device count while considering the operating conditions and limitations of the IC and all real external components. The ADIsimPower tool can be found at http://www.analog.com/ADIsimPower; the user can request an unpopulated board through the tool.

## PROGRAMMING THE OUTPUT VOLTAGE

The output voltage of the ADP5014 is externally set by a resistive voltage divider from the VREF pin to the VSETx pin and a resistive voltage divider from the output voltage to the FBx pin. To limit the degradation of the output voltage accuracy due to VSETx and FBx bias current, ensure the value of the bottom resistor in the dividers is not too large.

The ADP5014 provides adjustable output voltage settings. Use the resistor divider from the accurate internal $V_{REF}$ reference voltage (VREF pin) to set the desired output voltage and directly tie the FBx pin to the output when the desired output voltage setting is less than the $V_{REF}$ voltage, as shown in Figure 38. The equation for the output voltage setting is

$$V_{OUT} = V_{REF} \times (R_2/(R_1+R_2))$$

where:
$V_{OUT}$ is the output voltage.
$V_{REF}$ is the 2.0 V accurate low noise reference voltage.
$R_2$ is the resistor from VSETx to ground.
$R_1$ is the resistor from VSETx to $V_{REF}$.

If the desired output voltage exceeds the $V_{REF}$ voltage, use an external resistor divider from the output to the FBx pin to set the desired output voltage, and tie VSETx to VREF directly, as shown in Figure 39.

The equation for the output voltage setting is as follows:

$$V_{OUT} = V_{REF} \times (1 + (R_{TOP}/R_{BOT}))$$

where:
$V_{OUT}$ is the output voltage.
$V_{REF}$ is the 2.0 V accurate low noise reference voltage.
$R_{TOP}$ is the feedback resistor from $V_{OUT}$ to FB.
$R_{BOT}$ is the feedback resistor from FB to ground.

## VOLTAGE CONVERSION LIMITATIONS

For a given input voltage, lower limitations on the output voltage exist due to the minimum on time and the minimum off time.

The minimum output voltage for a given input voltage and switching frequency is limited by the minimum on time. The minimum on time for each channel is 60 ns (typical). The minimum on time increases at higher junction temperatures.

Note that in FPWM mode, the output voltage potentially exceeds the nominal output voltage when the minimum on time limit is reached. Careful switching frequency selection is required to avoid this problem.

The minimum output voltage in CCM mode for a given input voltage and switching frequency is calculated using the following equation:

$$V_{OUT\_MIN} = V_{IN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON1} - R_{DSON2}) \times I_{OUT\_MIN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON2} + R_L) \times I_{OUT\_MIN} \quad (1)$$

where:
$V_{OUT\_MIN}$ is the minimum output voltage.
$t_{MIN\_ON}$ is the minimum on time.
$f_{SW}$ is the switching frequency.
$R_{DSON1}$ is the high-side MOSFET on resistance.
$R_{DSON2}$ is the low-side MOSFET on resistance.
$I_{OUT\_MIN}$ is the minimum output current.
$R_L$ is the resistance of the output inductor.

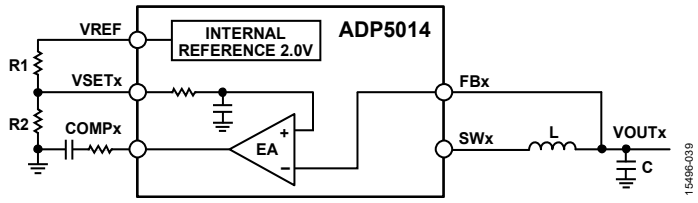



*Figure 38. Configure the Output Voltage when $V_{OUTx} \le V_{REF}$*

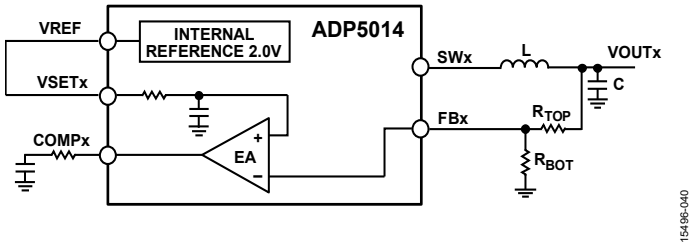



*Figure 39. Configure the Output Voltage when $V_{OUTx} > V_{REF}$*

The maximum output voltage for a given input voltage and switching frequency is limited by the minimum off time or the maximum duty cycle. The minimum off time for each channel is 50 ns (typical).

The maximum output voltage for a given input voltage and switching frequency is calculated using the following equation:

$$V_{OUT\_MAX} = V_{IN} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON1} - R_{DSON2}) \times I_{OUT\_MAX} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON2} + R_L) \times I_{OUT\_MAX} \quad (2)$$

where:
$V_{OUT\_MAX}$ is the maximum output voltage.
$t_{MIN\_OFF}$ is the minimum off time.
$f_{SW}$ is the switching frequency.
$R_{DSON1}$ is the high-side MOSFET on resistance.
$R_{DSON2}$ is the low-side MOSFET on resistance.
$I_{OUT\_MAX}$ is the maximum output current.
$R_L$ is the resistance of the output inductor.

As shown in Equation 1 and Equation 2, reducing the switching frequency eases the minimum on time and off time limitations.

## CURRENT-LIMIT SETTING

The ADP5014 has two selectable current-limit thresholds for each channel. Ensure that the selected current-limit value is larger than the peak current of the inductor, $I_{PEAK}$. See Table 6 for the current-limit configuration for each channel.

## SOFT START SETTING

The buck regulators in the ADP5014 include soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current. To set the soft start time to a value of 2 ms or 16 ms, connect a resistor from the CFG2 pin to the ground (see the Soft Start section).

## INDUCTOR SELECTION

The inductor value is determined by the operating frequency, input voltage, output voltage, and inductor ripple current. Using a small inductor yields faster transient response but degrades efficiency due to the larger inductor ripple current. Using a large inductor value yields a smaller ripple current and better efficiency, but results in slower transient response. Therefore, a trade-off must be made between the transient response and efficiency. As a guideline, the inductor ripple current, $\Delta I_L$, is typically set to a value from 30% to 40% of the maximum load current. The inductor value is calculated using the following equation:

$$L = [(V_{IN} - V_{OUT}) \times D]/(\Delta I_L \times f_{SW})$$

where:
$V_{IN}$ is the input voltage.
$V_{OUT}$ is the output voltage.
$D$ is the duty cycle ($D = V_{OUT}/V_{IN}$).
$\Delta I_L$ is the inductor ripple current.
$f_{SW}$ is the switching frequency.

The ADP5014 has internal slope compensation in the current loop to prevent subharmonic oscillations when the duty cycle is greater than 50%.The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{OUT} + (\Delta I_L/2)$$

The saturation current of the inductor must be larger than the peak inductor current. For ferrite core inductors with a fast saturation characteristic, the saturation current rating of the inductor are higher than the current-limit threshold of the buck regulator to prevent the inductor from becoming saturated.

The rms current of the inductor is calculated using the following equation:

$$I_{RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}}$$

Shielded ferrite core materials are recommended for low core loss and low electromagnetic interference (EMI). Table 11 lists the recommended inductors.

**Table 11. Recommended Inductors**

| Vendor | Part No. | Value (µH) | $I_{SAT}$ (A) | $I_{RMS}$ (A) | DCR (mΩ) | Size (mm) |
|---|---|---|---|---|---|---|
| Coilcraft | XAL4020-601 | 0.6 | 10.4 | 11.7 | 9.5 | 4 × 4 |
| | XAL4020-102 | 1.0 | 8.7 | 9.6 | 13.3 | 4 × 4 |
| | XAL4020-152 | 1.5 | 7.1 | 7.5 | 21.5 | 4 × 4 |
| | XAL4020-222 | 2.2 | 5.6 | 5.5 | 35.2 | 4 × 4 |
| TOKO | DFE252012P-R68M | 0.68 | 5.3 | 4.1 | 30 | 2.5 × 2.0 |
| | DFE252012P-1R0P | 1.0 | 4.8 | 3.8 | 35 | 2.5 × 2.0 |
| | DFE252012P-1R5P | 1.5 | 3.9 | 3.0 | 50 | 2.5 × 2.0 |
| | DFE252012P-2R2P | 2.2 | 3.4 | 2.6 | 70 | 2.5 × 2.0 |
| Wurth | 744383560068 | 0.68 | 9.4 | 8.2 | 7.5 | 4.1 × 4.1 |
| | 74438356010 | 1 | 9.0 | 7.2 | 12 | 4.1 × 4.1 |
| | 74438356015 | 1.5 | 7.8 | 5.8 | 15 | 4.1 × 4.1 |
| | 74438356022 | 2.2 | 6.2 | 4.7 | 29 | 4.1 × 4.1 |

## OUTPUT CAPACITOR SELECTION

The selected output capacitor affects both the output voltage ripple and the loop dynamics of the regulator. For example, during load step transients on the output, when the load is suddenly increased, the output capacitor supplies the load until the control loop can ramp up the inductor current, causing an undershoot of the output voltage.

The output capacitance required to meet the voltage droop requirement ($C_{OUT\_UV}$) is calculated using the following equation:

$$C_{OUT\_UV} = \frac{K_{UV} \times \Delta I_{STEP}{}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT\_UV}}$$

where:
$K_{UV}$ is a factor (typically set to 2).
$\Delta I_{STEP}$ is the load step.
$\Delta V_{OUT\_UV}$ is the allowable undershoot on the output voltage.

Another example of the effect of the output capacitor on the loop dynamics of the regulator is when the load is suddenly removed from the output. The energy stored in the inductor rushes into the output capacitor, causing an overshoot of the output voltage.

The output capacitance required to meet the overshoot requirement ($C_{OUT\_UV}$) is calculated using the following equation:

$$C_{OUT\_OV} = \frac{K_{OV} \times \Delta I_{STEP}{}^2 \times L}{(V_{OUT} + \Delta V_{OUT\_OV})^2 - V_{OUT}{}^2}$$

where:
$K_{OV}$ is a factor (typically set to 2).
$\Delta I_{STEP}$ is the load step.
$\Delta V_{OUT\_OV}$ is the allowable overshoot on the output voltage.

The output voltage ripple is determined by the equivalent series resistance (ESR) of the output capacitor and its capacitance value. Use the following equation to select a capacitor that can meet the output ripple requirements:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT\_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

where:
$\Delta V_{OUT\_RIPPLE}$ is the allowable output voltage ripple.
$R_{ESR}$ is the ESR of the output capacitor.

Select the largest output capacitance given by $C_{OUT\_UV}$, $C_{OUT\_OV}$, and $C_{OUT\_RIPPLE}$ to meet both load transient and output ripple requirements.

The selected output capacitor voltage rating must be greater than the output voltage. The minimum rms current rating of the output capacitor ($I_{COUT\_rms}$) is determined by the following equation:

$$I_{COUT\_rms} = \frac{\Delta I_L}{\sqrt{12}}$$

## INPUT CAPACITOR SELECTION

The input decoupling capacitor attenuates high frequency noise on the input and acts as an energy reservoir. This capacitor is a ceramic capacitor and must be placed close to the PVINx pins. The loop composed of the input capacitor, the high-side MOSFET, and the low-side MOSFET must be kept as small as possible. The voltage rating of the input capacitor must be greater than the maximum input voltage. The rms current rating of the input capacitor ($I_{CIN\_rms}$)is larger than the following equation:

$$I_{CIN\_rms} = I_{OUT} \times \sqrt{D\,(1 - D)}$$

where $D$ is the duty cycle ($D = V_{OUT}/V_{IN}$).

## PROGRAMMING THE UVLO INPUT

The precision enable input can be used to program the UVLO threshold of the input voltage, as shown in Figure 32.

The precision turn on threshold is 0.6 V. Use the following equations to calculate $R_{TOP\_EN}$ and $R_{BOT\_EN}$:

$$R_{TOP\_EN} = (0.57\ V \times V_{IN\_RISING} - 0.6 \times V_{IN\_FALLING})/(0.57\ V \times 4\ \mu A - 0.6 \times 1\ \mu A)$$

$$R_{BOT\_EN} = (0.6\ V \times R_{TOP\_EN})/(V_{IN\_RISING} - R_{TOP\_EN} \times 4\ \mu A - 0.6\ V)$$

where:
$R_{TOP\_EN}$ is the resistor from PVINx to ENx.
$V_{IN\_RISING}$ is the $V_{IN}$ rising threshold.
$V_{IN\_FALLING}$ is the $V_{IN}$ falling threshold.
$R_{BOT\_EN}$ is the resistor from ENx to ground.

## COMPENSATION COMPONENTS DESIGN

For the peak current-mode control architecture, the power stage can be simplified as a voltage controlled current source that supplies current to the output capacitor and load resistor. The simplified loop is composed of one domain pole and a zero contributed by the ESR of the output capacitor. The control to output transfer function ($G_{vd}$) is shown in the following equations:

$$G_{vd}(s) = \frac{V_{OUT}(s)}{V_{COMP}(s)} = A_{VI} \times R \times \frac{\left(1 + \frac{s}{2 \times \pi \times f_z}\right)}{\left(1 + \frac{s}{2 \times \pi \times f_p}\right)}$$

$$f_z = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

$$f_p = \frac{1}{2 \times \pi \times (R + R_{ESR}) \times C_{OUT}}$$

where:
$A_{VI}$ = 16.67A/V for Channel 1 or Channel 2, and 8.33 A/V for Channel 3 or Channel 4.
$R$ is the load resistance.
$f_z$ is the frequency of the zero.
$C_{OUT}$ is the output capacitance.
$R_{ESR}$ is the equivalent series resistance of the output capacitor.
$f_p$ is the frequency of the pole.

The ADP5014 uses a transconductance amplifier as the error amplifier to compensate the system. Figure 40 shows the simplified peak current-mode control small signal circuit.

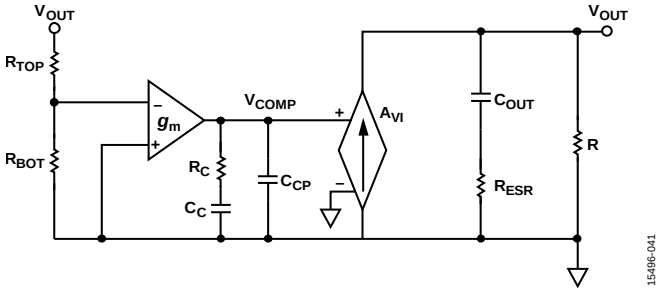



*Figure 40. Simplified Peak Current-Mode Control Small Signal Circuit*

The compensation components, $R_C$ and $C_C$, contribute a zero and the optional $C_{CP}$ and $R_C$ contribute an optional pole.

The closed-loop transfer ($T_V(s)$) equation is as follows:

$$T_V(s) = \frac{R_{BOT}}{R_{BOT}+R_{TOP}} \times \frac{-g_m}{C_C+C_{CP}} \times \frac{1+R_C \times C_C \times s}{s \times \left(1+\frac{R_C \times C_C \times C_{CP}}{C_C+C_{CP}} \times s\right)} \times G_{vd}(s)$$

The following procedure shows how to select the compensation components—$R_C$, $C_C$, and $C_{CP}$,—for ceramic output capacitor applications.

1. Determine the cross frequency ($f_C$). Generally, $f_C$ is between $f_{SW}/12$ and $f_{SW}/6$.
2. $R_C$ can be calculated using the following equation:

$$R_C = \frac{2 \times \pi \times V_{OUT} \times C_{OUT} \times f_C}{VSETx \times g_m \times A_{VI}}$$

3. Place the compensation zero at the domain pole ($f_P$). $C_C$ can be determined as follows:

$$C_C = \frac{\left(R+R_{ESR}\right) \times C_{OUT}}{R_C}$$

4. $C_{CP}$ is optional. It can be used to cancel the zero caused by the ESR of the output capacitor.

$$C_{CP} = \frac{R_{ESR} \times C_{OUT}}{R_C}$$

## POWER DISSIPATION

The total power dissipation in the ADP5014 ($P_D$) simplifies to

$$P_D = P_{BUCK1} + P_{BUCK2} + P_{BUCK3} + P_{BUCK4}$$

### *Buck Regulator Power Dissipation*

The power dissipation ($P_{LOSS}$) for each buck regulator includes power switch conductive losses ($P_{COND}$), switch losses ($P_{SW}$), and transition losses ($P_{TRAN}$). Other sources of power dissipation exist, but these sources are generally less significant at the high output currents of the application thermal limit.

Use the following equation to estimate the power dissipation of the buck regulator:

$$P_{LOSS} = P_{COND} + P_{SW} + P_{TRAN}$$

#### Power Switch Conduction Loss ($P_{COND}$)

Power switch conduction losses are caused by the flow of output current through both the high-side and low-side power switches, each of which has on resistance ($R_{DS(ON)}$).

Use the following equation to estimate the power switch conduction loss:

$$P_{COND} = (R_{DS(ON)\_HS} \times D + R_{DS(ON)\_LS} \times (1 - D)) \times I_{OUT}^2$$

where:
$R_{DS(ON)\_HS}$ is the high-side MOSFET on resistance.
$R_{DS(ON)\_LS}$ is the low-side MOSFET on resistance.
$D$ is the duty cycle ($D = V_{OUT}/V_{IN}$).

#### Switching Loss ($P_{SW}$)

Switching losses are associated with the current drawn by the driver to turn the power devices on and off at the switching frequency. Each time a power device gate is turned on or off, the driver transfers a charge from the input supply to the gate, and then from the gate to ground. Use the following equation to estimate the switching loss:

$$P_{SW} = (C_{GATE\_HS} + C_{GATE\_LS}) \times V_{IN}^2 \times f_{SW}$$

where:
$C_{GATE\_HS}$ is the gate capacitance of the high-side switch.
$C_{GATE\_LS}$ is the gate capacitance of the low-side switch.
$f_{SW}$ is the switching frequency.

#### Transition Loss ($P_{TRAN}$)

Transition losses occur because the high-side switch cannot turn on or off instantaneously. During a switch node transition, the power switch provides all the inductor current. The source to drain voltage of the power switch is half the input voltage, resulting in power loss. Transition losses increase with both load and input voltage and occur twice for each switching cycle. Use the following equation to estimate the transition loss:

$$P_{TRAN} = 0.5 \times V_{IN} \times I_{OUT} \times (t_R + t_F) \times f_{SW}$$

where:
$t_R$ is the rise time of the switch node.
$t_F$ is the fall time of the switch node.

#### Thermal Shutdown

When the ADP5014 operates under a heavy load in a high ambient temperature, the power loss can cause the junction temperature to exceed the maximum junction temperature of 125°C. If the junction temperature exceeds 150°C, the regulator enters thermal shutdown and recovers when the junction temperature falls below 135°C.

## JUNCTION TEMPERATURE

The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to power dissipation, as shown in the following equation:

$$T_J = T_A + T_R$$

where:
$T_J$ is the junction temperature.
$T_A$ is the ambient temperature.
$T_R$ is the rise in temperature of the package due to power dissipation.

The rise in temperature of the package is directly proportional to the power dissipation in the package. The proportionality constant for this relationship is the thermal resistance from the junction of the die to the ambient temperature, as shown in the following equation:

$$T_R = \theta_{JA} \times P_D$$

where:
$T_R$ is the rise in temperature of the package.
$\theta_{JA}$ is the thermal resistance from the junction of the die to the ambient temperature of the package (see Table 4). Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.
$P_D$ is the power dissipation in the package.An important factor to consider is that the thermal resistance value is based on a 4-layer, 4 inch × 3 inch PCB with 2.5 oz of copper, as specified in the JEDEC standard, whereas real world applications can use PCBs with different dimensions and a different number of layers.

It is important to maximize the amount of copper used to remove heat from the device. Copper exposed to air dissipates heat better than copper used in the inner layers. The exposed pad is connected to the ground plane with several vias.

# DESIGN EXAMPLES

This section provides an example of the step by step design procedures and the external components required for Channel 1. Table 12 lists the design requirements for this example.

**Table 12. Example Design Requirements for Channel 1**

| Parameter | Specification |
|---|---|
| Input Voltage | $V_{PVIN1}$ = 5 V ± 5% |
| Output Voltage | $V_{OUT1}$ = 1.2 V |
| Output Current | $I_{OUT1}$ = 4 A |
| Output Ripple | $\Delta V_{OUT1\_RIPPLE}$ = 5 mV in CCM mode |
| Load Transient | ±5%, at 20% to 80% load transient, 1 A/µs |

Although this example shows step by step design procedures for Channel 1, the procedures apply to all other buck regulator channels (Channel 2 to Channel 4).

## SETTING THE SWITCHING FREQUENCY

The first step when setting the switching frequency is to determine the switching frequency for the ADP5014 design. In general, higher switching frequencies produce a smaller solution size due to the lower component values required, whereas lower switching frequencies result in higher conversion efficiency due to lower switching losses.

The switching frequency of the ADP5014 can be set to a value from 500 kHz to 2.5 MHz by connecting a resistor from the RT pin to ground. The selected resistor allows users to make decisions based on the trade-off between efficiency and solution size. For more information, see the Oscillator section.

However, the highest supported switching frequency must be assessed by checking the voltage conversion limitations enforced by the minimum on time and the minimum off time (see the Voltage Conversion Limitations section).

In this design example, a switching frequency of 1.2 MHz achieves a good combination of small solution size and high conversion efficiency. To set the switching frequency to 1.2 MHz, use the following equation to calculate the resistor value, $R_{RT}$:

$$R_{RT}\ (\text{k}\Omega) = (100{,}000/f_{SW}\ (\text{kHz}))$$

According to this equation, select standard resistor $R_{RT}$ = 82.5 kΩ.

## SETTING THE OUTPUT VOLTAGE

Because the desired output voltage setting is less than $V_{REF}$ voltage, use the resistor divider from the accurate internal VREF reference voltage to set the desired output voltage and directly tie the feedback pin (FB1) to the output (see Figure 38). Select a 10 kΩ bottom resistor (R2) and then calculate the top resistor using the following equation:

$$R1 = R2 \times ((V_{REF} - V_{OUT})/V_{OUT})$$

where:
$V_{OUT}$ is the output voltage.
$V_{REF}$ is 2.0 V for Channel 1 to Channel 4.

To set the output voltage to 1.2 V, choose the following resistor values: R1 = 6.65 kΩ, and R2 = 10 kΩ.

## SETTING THE CONFIGUATIONS (CFG1 AND CFG2)

The CFG1 pin can be used to program the load output capability and parallel operation for all channels. For this example, choose $R_{CFG1}$ = 0 kΩ. For more information, see the configuration in Function Configurations (CFG1 and CFG2).

The CFG2 pin can be used to program the operation mode (FPWM or PWM/PSM mode), the enable mode (manual mode or sequence mode), the timer (×1 or ×8), and GPIO functionalities (PWRGD, SYNC-IN, CLK-OUT, UVO) for all channels. For this example, choose $R_{CFG2}$ = 0 kΩ. For more information, see the configuration in Function Configurations (CFG1 and CFG2).

## SELECTING THE INDUCTOR

The peak-to-peak inductor ripple current, $\Delta I_L$, is set to 30% of the maximum output current. Use the following equation to estimate the value of the inductor (L):

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

where:
$V_{IN}$ = 5 V.
$V_{OUT}$ = 1.2 V.
$D$ is the duty cycle ($D = V_{OUT}/V_{IN}$ = 0.24).
$\Delta I_L$ = 30% × 4 A = 1.2 A.
$f_{SW}$ = 1.2 MHz.

The resulting value for L is 0.63 µH. The closest standard inductor value is 0.8 µH; therefore, the inductor ripple current, $\Delta I_{L1}$, is 0.95 A.

The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{OUT} + (\Delta I_L/2)$$

The calculated peak current for the inductor is 4.48 A.

The rms current of the inductor can be calculated using the following equation:

$$I_{RMS} = \sqrt{{I_{OUT}}^2 + \frac{{\Delta I_L}^2}{12}}$$

The rms current of the inductor is approximately 4.01 A. Therefore, an inductor with a minimum rms current rating of 4.01 A and a minimum saturation current rating of 4.48 A is required. However, to prevent the inductor from reaching its saturation point in current-limit conditions, it is recommended that the inductor saturation current be higher than the maximum peak current limit, typically 6 A, for reliable operation.

Based on these requirements and recommendations, the COILCRAFT XAL5030-801MEB, with a direct current resistance (DCR) of 5.14 mΩ, is selected for this design.

## SELECTING THE OUTPUT CAPACITOR

The output capacitor must meet the output voltage ripple and load transient requirements. To meet the output voltage ripple requirement, use the following equation to calculate the ESR and capacitance:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT\_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

The calculated capacitance, $C_{OUT\_RIPPLE}$, is 19.8 µF, and the calculated $R_{ESR}$ is 5 mΩ.

To meet the ±5% overshoot and undershoot requirements, use the following equations to calculate the capacitance:

$$C_{OUT\_UV} = \frac{K_{UV} \times \Delta I_{STEP}{}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT\_UV}}$$

$$C_{OUT\_OV} = \frac{K_{OV} \times \Delta I_{STEP}{}^2 \times L}{(V_{OUT} + \Delta V_{OUT\_OV})^2 - V_{OUT}{}^2}$$

For estimation purposes, use $K_{OV} = K_{UV} = 2$; therefore, $C_{OUT\_OV} = 62.4$ µF and $C_{OUT\_UV} = 20.2$ µF.

The ESR of the output capacitor must be less than 5 mΩ, and the output capacitance must be greater than 62.4 µF. It is recommended that two ceramic capacitors be used (47 µF, X5R, 6.3 V), such as the GRM21BR60J476ME15 from Murata with an ESR of 2 mΩ.

## DESIGNING THE COMPENSATION NETWORK

For better load transient and stability performance, set the cross frequency, $f_C$, to $f_{SW}/10$. In this example, $f_{SW}$ is set to 1.2 MHz; therefore, $f_C$ is set to 120 kHz.

For the 1.2 V output rail, the 47 µF ceramic output capacitor has a derated value of 32 µF.

$$R_C = \frac{2 \times \pi \times 1.2\,V \times 2 \times 32\,\mu F \times 120\,kHz}{1.2\,V \times 800\,\mu s \times 16.67\,A/V} = 3.62\,k\Omega$$

$$C_C = \frac{(0.3\,\Omega + 0.001\,\Omega) \times 2 \times 32\,\mu F}{3.62\,k\Omega} = 5.32\,nF$$

$$C_{CP} = \frac{0.001\,\Omega \times 2 \times 32\,\mu F}{3.62\,k\Omega} = 17.7\,pF$$

Choose standard components: $R_C = 3.57$ kΩ and $C_C = 5.6$ nF. $C_{CP}$ is optional.

Figure 41 shows the bode plot for the 1.2 V output rail. The cross frequency is 132 kHz, and the phase margin is 56°. The load transient waveform is shown in Figure 42.

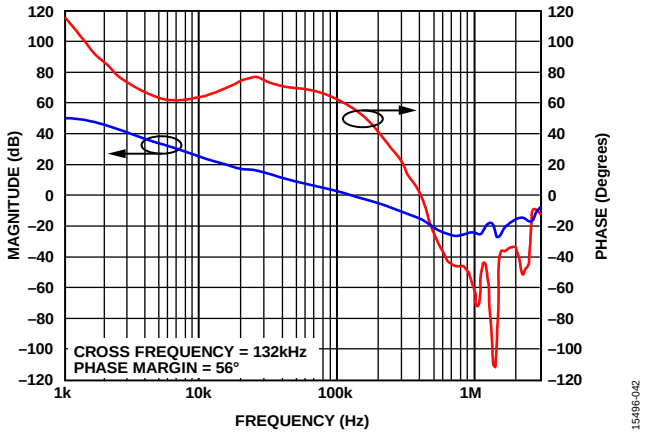



Figure 41. Bode Plot for 1.2 V Output

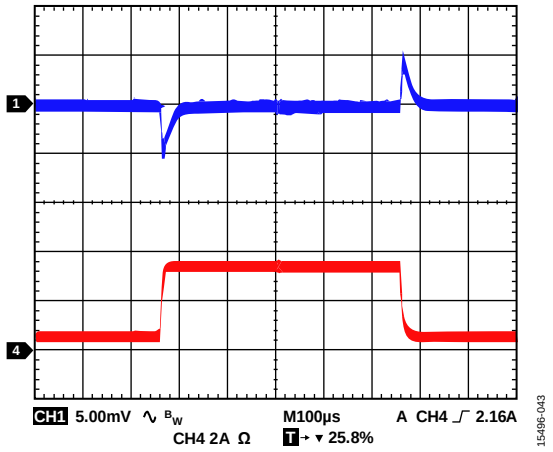



Figure 42. Selecting the Input Capacitor

For the input capacitor, select a ceramic capacitor with a minimum value of 10 µF. The input capacitor is placed close to the PVINx pin. In this example, one ceramic capacitor of 10 µF, X5R, 16 V is recommended.

## LOW NOISE OUTPUT DESIGN

The ADP5014 optimizes many analog blocks and uses new unity-gain reference architecture to achieve lower output noise in low-frequency range. When the system design needs the low noise output of ADP5014 , the device enables powering up the signal chain products directly without LDOs. In this scenario, adding an additional LC filter is highly recommended after the main LC filter to filter the fundamental switching ripple and its harmonic. This is because the switching ripples may generate unexpected noise spurs for the noises sensitive signal chain devices. Because this additional inductor filter may generate voltage drop at the load, the inductor with small DCR is recommended to minimize the voltage drop, especially for high current applications.

Figure 43 and Figure 44 show the ADP5014 noise spectral density measurement from a 10 Hz to 10 MHz frequency range and integrated rms noise from a 10 Hz to 1 MHz frequency range, compared to the ADP1740 as another traditional, 2 A, low noise linear regulator.

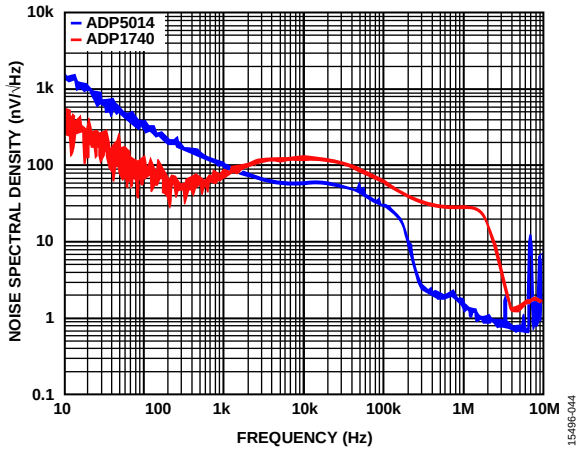



*Figure 43. ADP5014 Noise Spectral Density Measurement, $V_{IN}$ = 5 V, $V_{OUT1}$ = 1.3 V, $I_{OUT1}$ = 0.5 A, $f_{SW}$ = 1.2 MHz, $L_1$ = 0.8 µH, $C_{OUT}$ = 47 µF × 3, $L_{FILTER}$ = 1 µH, $C_{FILTER}$ = 22 µF × 2*

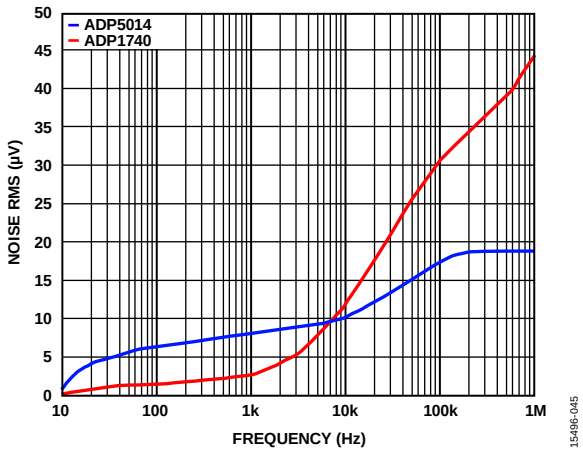



*Figure 44. ADP5014 Integrated RMS Noise, $V_{IN}$ = 5 V, $V_{OUT1}$ = 1.3 V, $I_{OUT1}$ = 0.5 A, $f_{SW}$ = 1.2 MHz, $L_1$ = 0.8 µH, $C_{OUT}$ = 47 µF × 3, $L_{FILTER}$ = 1 µH, $C_{FILTER}$ = 22 µF × 2*

# PCB LAYOUT RECOMMENDATIONS

Good circuit board layout is essential to obtain the best performance from the ADP5014 (see Figure 45). Poor layout can affect the regulation and stability of the device, as well as the EMI and electromagnetic compatibility (EMC) performance. Refer to the following guidelines for a good PCB layout.

- Place the input capacitor, inductor, and output capacitor close to the IC.
- Use short, thick traces to connect the input capacitors to the PVINx pins, and use dedicated power ground to connect the input and output capacitor grounds to minimize the connection length.
- Use several high current vias, if required, to connect PVINx, PGNDx, or SWx to other power planes.
- Use short, thick traces to connect the inductors to the SWx pins and the output capacitors.
- Ensure that the high current loop traces are as short and wide as possible.
- Maximize the amount of ground metal for the exposed pad, and use as many vias as possible on the component side to improve thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.
- Place the decoupling capacitors close to the VREF pin.
- Place the RC filter close to the AVIN pin.
- Place the frequency setting resistor close to the RT pin.
- Place the $V_{REF}$ resistor divider close to the VSETx and the feedback resistor divider close to the FBx pin. In addition, keep the VSETx and FBx traces away from the high current traces and the switch node to avoid noise pickup.
- Use size 0402 or 0603 resistors and capacitors to achieve the smallest possible footprint solution on boards where space is limited.

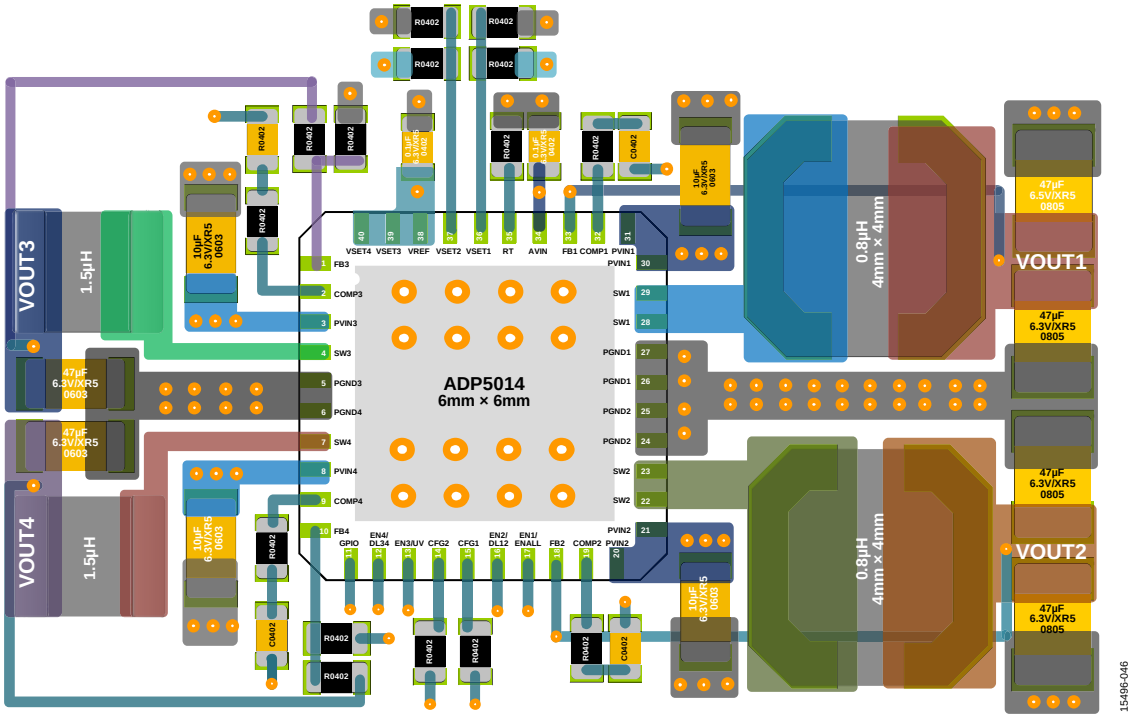



*Figure 45. Typical PCB Layout for the ADP5014*

# TYPICAL APPLICATION CIRCUITS

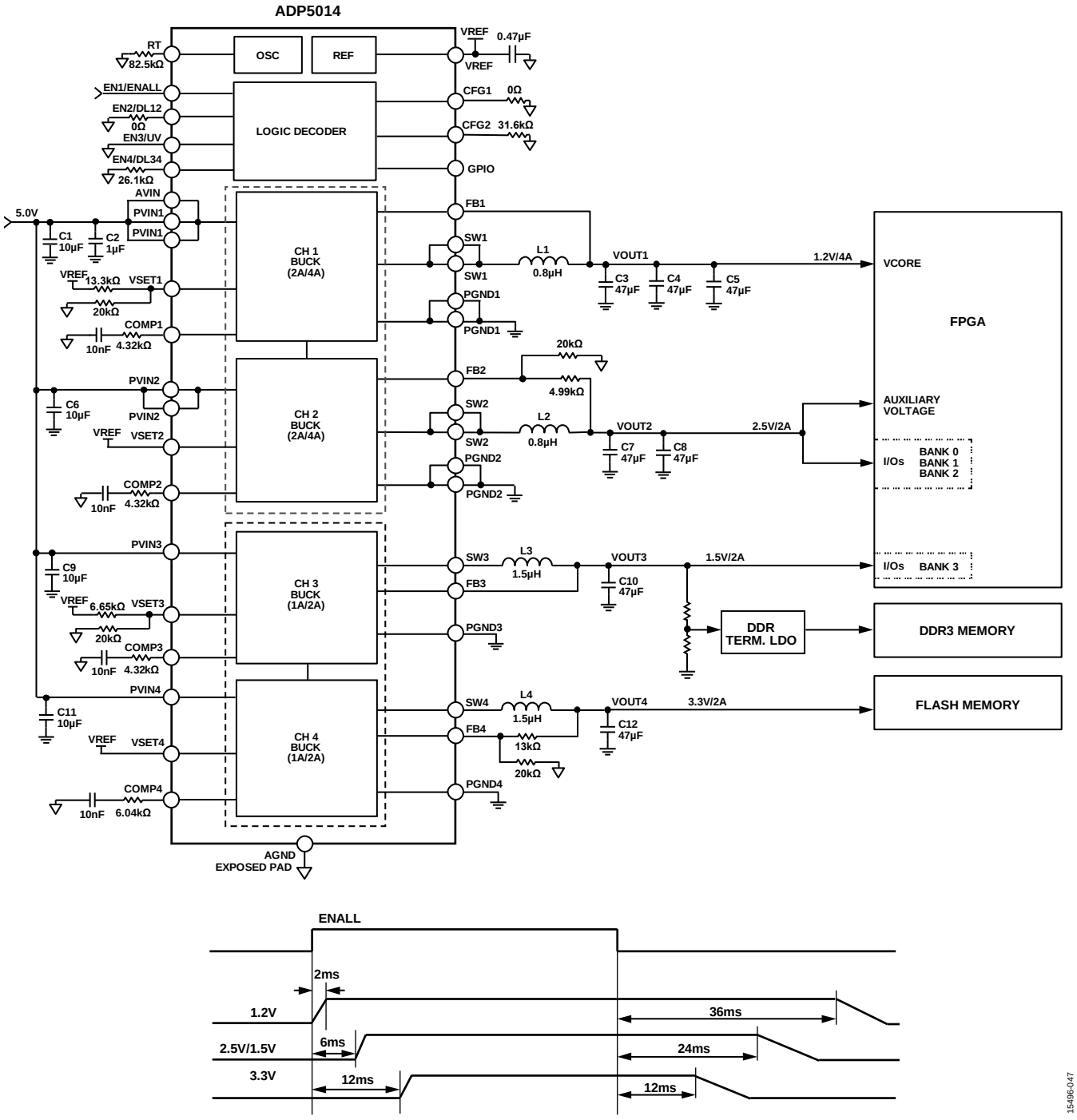



*Figure 46. Typical Field Programmable Gate Array (FPGA) Application, 1.2 MHz Switching Frequency, Sequence Enable Mode*

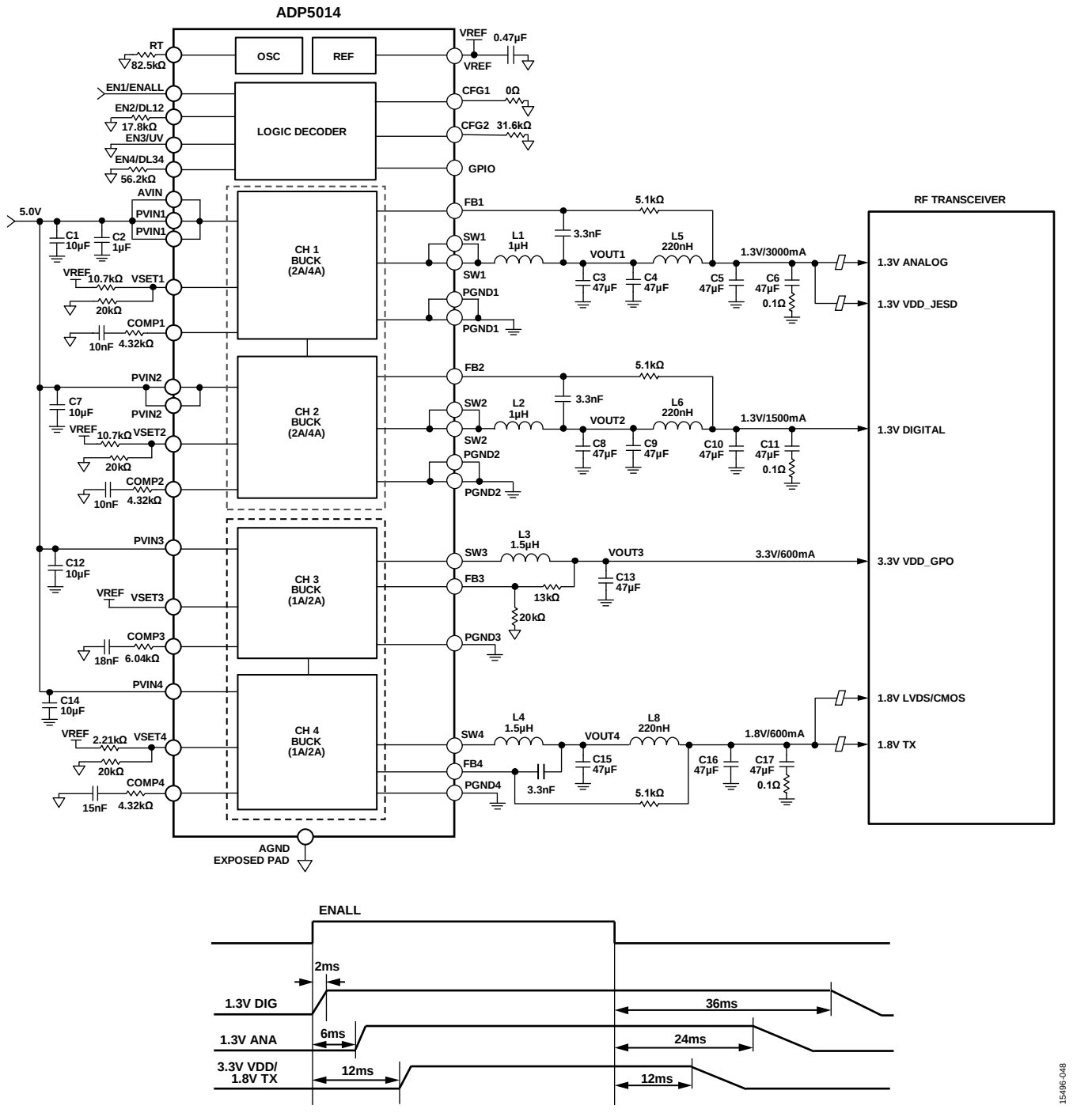



*Figure 47. Typical RF Transceiver Application, 1.2 MHz Switching Frequency, Sequence Enable Mode*

# FACTORY PROGRAMMABLE OPTIONS

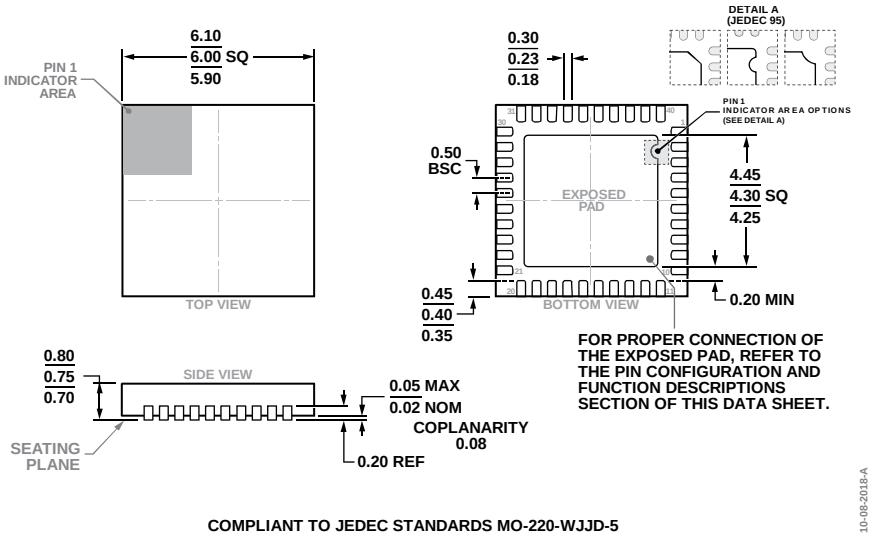
## FACTORY DEFAULT OPTIONS

Table 13 lists the factory default options programmed into the ADP5014 when the device is ordered (see the Ordering Guide). To order the device with options other than the default options, contact your local Analog Devices sales or distribution representative.

**Table 13. Factory Default Options**

| Option | Default Value |
|---|---|
| Channel 1 Output Voltage | Adjustable output |
| Channel 2 Output Voltage | Adjustable output |
| Channel 3 Output Voltage | Adjustable output |
| Channel 4 Output Voltage | Adjustable output |
| PWRGD Pin Output | Monitor all Channel 4 outputs (enabled by the CFG2 configuration) |
| Output Discharge Function | Enabled for all four buck regulators |
| Hiccup Detection | Hiccup protection enabled for overcurrent events |

# OUTLINE DIMENSIONS




**COMPLIANT TO JEDEC STANDARDS MO-220-WJJD-5**

*Figure 48. 40-Lead Lead Frame Chip Scale Package [LFCSP]*
*6 mm × 6 mm Body, and 0.75 mm Package Height*
*(CP-40-10)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option[2] |
|---|---|---|---|
| ADP5014ACPZ-R7 | −40°C to +125°C | 40-Lead Lead Frame Chip Scale Package [LFCSP] | CP-40-10 |
| ADP5014-EVALZ | | Evaluation Board | |

[1] Z = RoHS Compliant Part.
[2] Table 13 lists the factory default options for the device. For a list of factory programmable options, see the Factory Programmable Options section. To order a device with options other than the default values, contact your local Analog Devices sales or distribution representative.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