TPS6273x Step-Down Converter With Bypass Mode for Ultra Low-Power Wireless Applications

1 Features

- Input Voltage Range V_{IN} From 1.9 V to 3.9 V
- Typ. 30-nA Ultra Low-Power Bypass Mode
- Typ. 25-μA DC-DC Quiescent Current
- Internal Feedback Divider Disconnect
- Typical 2.1-Ω Bypass Switch Between V_{IN} and V_{OUT}
- Automatic Transition from DC-DC to Bypass Mode
- Up to 3-MHz Switch Frequency
- Up to 95% DC-DC Efficiency
- Open-Drain Status Output STAT
- Output Peak Current up to 100 mA
- Fixed Output Voltages 1.9 V, 2.05 V, 2.1 V, 2.3 V
- Small External Output Filter Components 2.2 μH and 2.2 μF
- Optimized For Low Output Ripple Voltage
- Small 1 × 1.5 × 0.6-mm^3 USON Package
- 12-mm^2 Minimum Solution Size

2 Applications

- CC2540 *Bluetooth*™ Low-Energy System-On-Chip Solution
- Low-Power Wireless Applications
- RF4CE, Metering

3 Description

The TPS62730 is a high frequency synchronous step-down DC-DC converter optimized for ultra low-power wireless applications. The device is optimized to supply TI's Low-Power Wireless sub 1-GHz and 2.4-GHz RF transceivers and System-On-Chip (SoC) solutions. The TPS62730 reduces the current consumption drawn from the battery during TX and RX mode by a high efficient step-down voltage conversion. The device provides an output current of up to 100 mA and allows the use of tiny and low-cost chip inductors and capacitors. With an input voltage range of 1.9 V to 3.9 V, the device supports Li-primary battery chemistries such as Li-SOCl2, Li-SO2, Li-MnO2, and also two cell alkaline batteries.

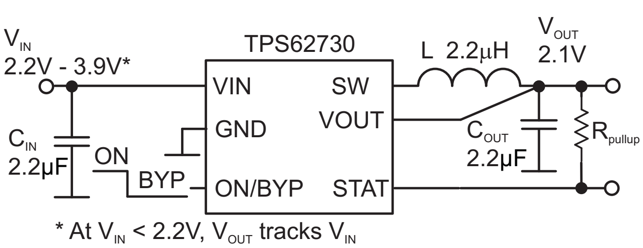
The TPS62730 features an Ultra Low-Power bypass mode with typical 30-nA current consumption to support sleep and low power modes of TI's CC2540 *Bluetooth* Low Energy and CC430 SoC solutions. In this bypass mode, the output capacitor of the DC-DC converter is connected through an integrated typical 2.1-Ω bypass switch to the battery.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62730	USON (6)	1.45 mm x 1.00 mm
TPS62732		
TPS62733		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



Battery Current Reduction Using TPS62730

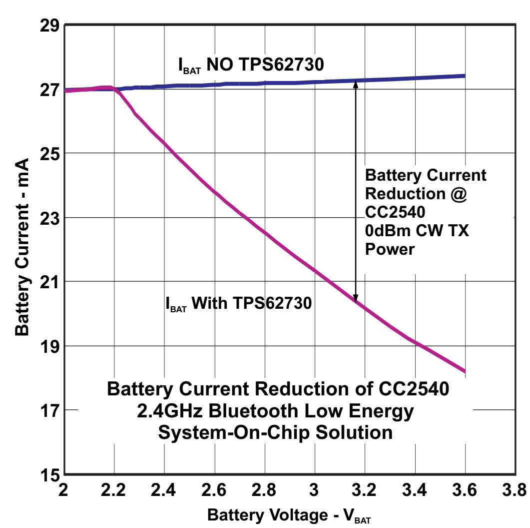


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Table of Contents

4 Revision History

Changes from Revision C (December 2012) to Revision D — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

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5 Description (Continued)

In DC-DC operation mode the device provides a fixed output voltage to the system. With a switch frequency up to 3 MHz, the TPS62730 features low output ripple voltage and low noise even with a small 2.2-uF output capacitor. The automatic transition into bypass mode during DC-DC operation prevents an increase of output ripple voltage and noise once the DC-DC converter operates close to 100% duty cycle. The device automatically enters bypass mode once the battery voltage falls below the transition threshold $V_{IT\ BYP}$. The TPS62730 is available in a 1 × 1.5-mm^2 6-pin USON package.

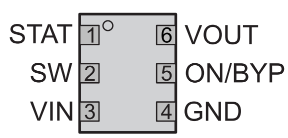
6 Device Comparison Table

T_A	PART NUMBER	OUTPUT VOLTAGE [V]	AUTOMATIC BYPASS MODE TRANSITION THRESHOLDS $V_{IT\ BYP}$		
			$V_{IT\ BYP}$ [V] RISING V_{IN}	$V_{IT\ BYP}$ [V] FALLING V_{IN}	$V_{IT\ BYP}$ [mV] HYSTERESIS
–40°C to 85°C	TPS62730	2.10	2.25	2.20	50
	TPS62731 (1)	2.05	2.2	2.15	50
	TPS62732	1.90	2.10	2.05	50
	TPS62733	2.3	2.48	2.41	70
	TPS62734 (1)	2.10	2.28	2.23	50
	TPS62735 (1)	2.10	2.33	2.23	100

(1) Device status is product preview. Contact TI for more details / samples.

7 Pin Configuration and Functions

DRY Package
6 Pins
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO		
VIN	3	PWR	V_{IN} power supply pin. Connect this pin close to the VIN terminal of the input capacitor. A ceramic capacitor of 2.2 µF is required.
GND	4	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor.
ON/BYP	5	IN	This is the mode selection pin of the device. Pulling this pin to low forces the device into ultra low-power bypass mode. The output of the DC-DC converter is connected to VIN through an internal bypass switch. Pulling this pin to high enables the DC-DC converter operation. This pin must be terminated and is controlled by the system.
SW	2	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the inductor to this terminal.
VOUT	6	IN	Feedback Pin for the internal feedback divider network and regulation loop. The internal bypass switch is connected between this pin and VIN. Connect this pin directly to the output capacitor with short trace.
STAT	1	OUT	This is the open-drain status output with active low level. An internal comparator drives this output. The pin is high impedance with ON/BYP = low. With ON/BYP set to high the device and the internal VOUT comparator becomes active. The active low STAT pin indicates if the DC-DC regulator is settled and the output voltage above the V_{TSTAT} threshold. If not used, this pin can be left open.

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8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, SW, VOUT	–0.3	4.2	V
	ON/BYP, STAT	–0.3	V_{IN} + 0.3 ≤ 4.2	V
Operating junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground pin.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM), all pins	±150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

8.3 Recommended Operating Conditions

Operating ambient temperature T_A = –40 to 85°C (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage V_{IN}	1.9		3.9	V
Effective inductance	1.5	2.2	3	µH
Effective output capacitance connected to V_{OUT}	1.0		10	µF
Operating junction temperature range, T_J	–40		125	°C
T_A Operating free air temperature range	-40		85	

8.4 Thermal Information

THERMAL METRIC(1)		TPS6273x DRY 6 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	293.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	165.1	
θ_{JB}	Junction-to-board thermal resistance	160.8	
ψ_{JT}	Junction-to-top characterization parameter	27.3	
ψ_{JB}	Junction-to-board characterization parameter	159.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	65.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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8.5 Electrical Characteristics

V_{IN} = 3.0 V, V_{OUT} = 2.1 V, ON/BYP = V_{IN}, T_A = –40°C to 85°C typical values are at T_A = 25°C (unless otherwise noted), C_{IN} = 2.2 µF, L = 2.2 µH, C_{OUT} = 2.2 µF

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY								
V_{IN}	Input voltage range				1.9		3.9	V
I_Q	Operating quiescent current		ON/BYP = high, I_{OUT} = 0mA. V_{IN} = 3 V device not switching			25	40	µA
			I_{OUT} = 0 mA. device switching, V_{IN} = 3.0 V, V_{OUT} = 2.1 V			34		
			ON/BYP = high, Bypass switch active, V_{IN} = V_{OUT} = 2.1 V			23		
I_{SD}	Shutdown current, Bypass Switch Activated(1)		ON/BYP = GND, leakage current into V_{IN}			30	550	nA
			ON/BYP = GND, leakage current into V_{IN}, T_A = 60°C			110		
ON/BYP								
$V_{IH\ TH}$	Threshold for detecting high ON/BYP		1.9 V ≤ V_{IN} ≤ 3.9 V , rising edge			0.8	1	V
$V_{IL\ TH}$	Threshold for detecting low ON/BYP		1.9 V ≤ V_{IN} ≤ 3.9 V , falling edge		0.4	0.6		V
I_{IN}	Input bias Current					0	50	nA
POWER SWITCH								
$R_{DS(ON)}$	High side MOSFET on-resistance		V_{IN} = 3.0 V			600		mΩ
	Low Side MOSFET on-resistance					350		
I_{LIMF}	Forward current limit MOSFET high side		V_{IN} = 3.0 V, open loop			410		mA
	Forward current limit MOSFET low side					410		mA
BYPASS SWITCH								
$R_{DS(ON)}$	Bypass Switch on-resistance		V_{IN} = 2.1 V, I_{OUT} = 20 mA, $T_J$max = 85°C			2.9	3.8	Ω
			V_{IN} = 3 V			2.1		
$V_{IT\ BYP}$	Automatic Bypass Switch Transition Threshold (Activation / Deactivation)	ON/BYP = high	TPS62730 (2.1 V)	ON / falling V_{IN}	2.14	2.20	2.3	V
				OFF/ rising V_{IN}	2.19	2.25	2.35	
			TPS62731 (2.05 V)	ON / falling V_{IN}		2.15		
				OFF / rising V_{IN}		2.20		
			TPS62732 (1.9 V)	ON / falling V_{IN}		2.05		
				OFF / rising V_{IN}		2.10		
			TPS62733 (2.3 V)	ON / falling V_{IN}		2.41		
				OFF/ rising V_{IN}		2.48		
			TPS62734 (2.1 V)	ON / falling V_{IN}		2.23		
				OFF / rising V_{IN}		2.28		
			TPS62735 (2.3 V)	ON / falling V_{IN}		2.23		
				OFF / rising V_{IN}		2.33		

(1) Shutdown current into VIN pin, includes internal leakage

Electrical Characteristics (continued)

V_{IN} = 3.0 V, V_{OUT} = 2.1 V, ON/BYP = V_{IN}, T_A = –40°C to 85°C typical values are at T_A = 25°C (unless otherwise noted), C_{IN} = 2.2 μF, L = 2.2 μH, C_{OUT} = 2.2 μF

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
STAT STATUS OUTPUT (OPEN DRAIN)							
V_{TSTAT}	Threshold level for STAT OUTPUT in % from V_{OUT}	ON/BYP = high and regulator is ready, V_{IN} falling			95%		
		ON/BYP = high and regulator is ready, V_{IN} rising[2]			98%		
V_{OL}	Output Low Voltage	Current into STAT pin I = 500 μA, V_{IN} = 2.3 V				0.4	V
V_{OH}	Output High Voltage	Open drain output, external pull up resistor				V_{IN}	
I_{LKG}	Leakage into STAT pin	ON/BYP = GND, V_{IN} = V_{OUT} = 3 V			0	50	nA
REGULATOR							
t_{ONmin}	Minimum ON time	V_{IN} = 3.0 V, V_{OUT} = 2.1 V, I_{OUT} = 0 mA			180		ns
t_{OFFmin}	Minimum OFF time	V_{IN} = 2.3 V			50		ns
t_{Start}	Regulator start up time from transition ON/BYP = high to STAT = low	V_{IN} = 3.0 V, V_{OUT} = 3.0 V			50		μs
OUTPUT							
V_{REF}	Internal Reference Voltage				0.70		V
V_{VOUT}	VOUT Feedback Voltage Comparator Threshold Accuracy	V_{IN} = 3.0 V	T_A = 25°C	–1.5%	0%	1.5%	
			T_A = –40°C to 85°C	–2.5%	0%	2.5%	
	DC output voltage load regulation	I_{OUT} = 1 mA to 50 mA V_{IN} = 3.0 V, V_{OUT} = 2.1 V			-0.01		%/mA
	DC output voltage line regulation	I_{OUT} = 20 mA, 2.4 V ≤ V_{IN} ≤ 3.9 V			0.01		%/V
I_{LK_SW}	Leakage current into SW pin	V_{IN} = V_{OUT} = V_{SW} = 3.0 V, ON/Byp= GND[3]			0.0	100	nA

(2) The STAT output comparator is enabled once the rising input voltage exceeds the minimum input voltage V_{IN} min of 1.9 V. In case of the 1.9 V output voltage option, the STAT output is active once the rising input voltage V_{IN} exceeds 1.9 V.
(3) The internal resistor divider network is disconnected from VOUT pin.

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8.6 Typical Characteristics

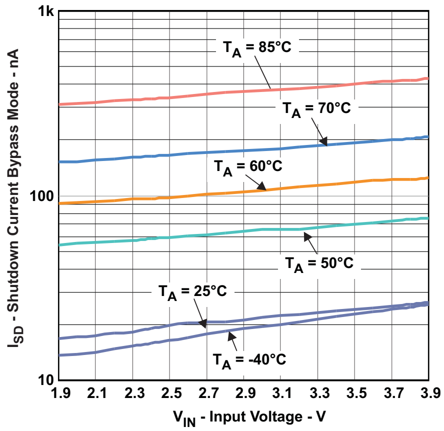


Figure 1. Shutdown Current Bypass Mode vs Input Voltage

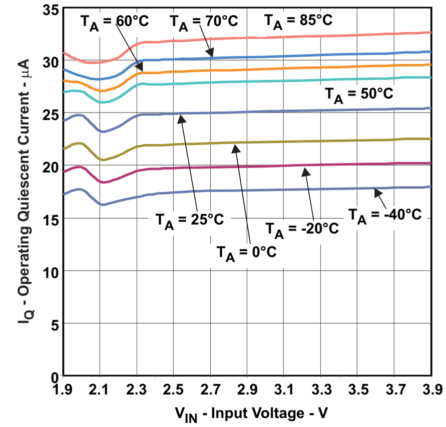


Figure 2. Operating Quiescent Current vs Input Voltage

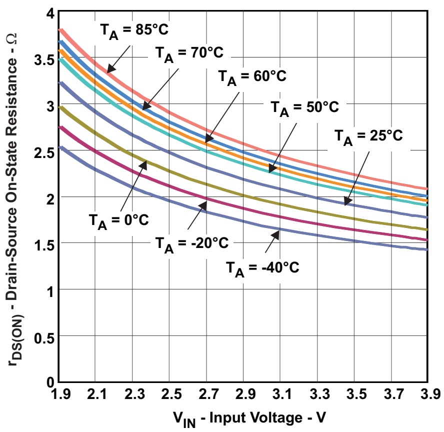


Figure 3. $r_{DS(ON)}$ Bypass vs Input Voltage

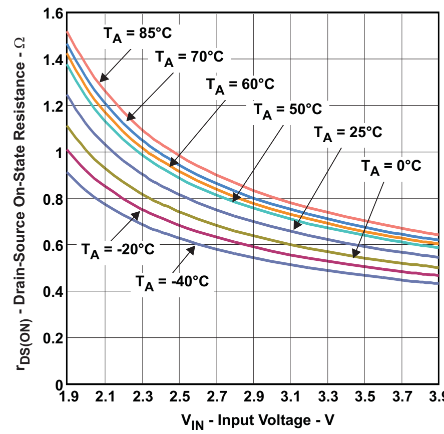


Figure 4. $r_{DS(ON)}$ PMOS vs Input Voltage

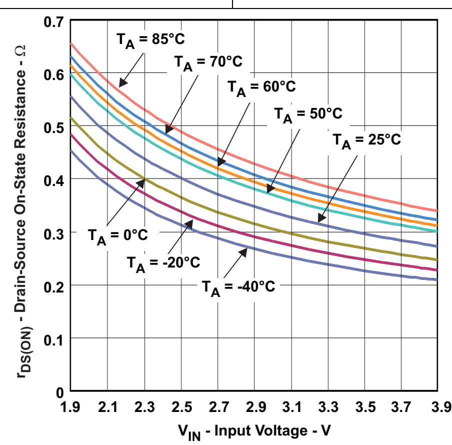


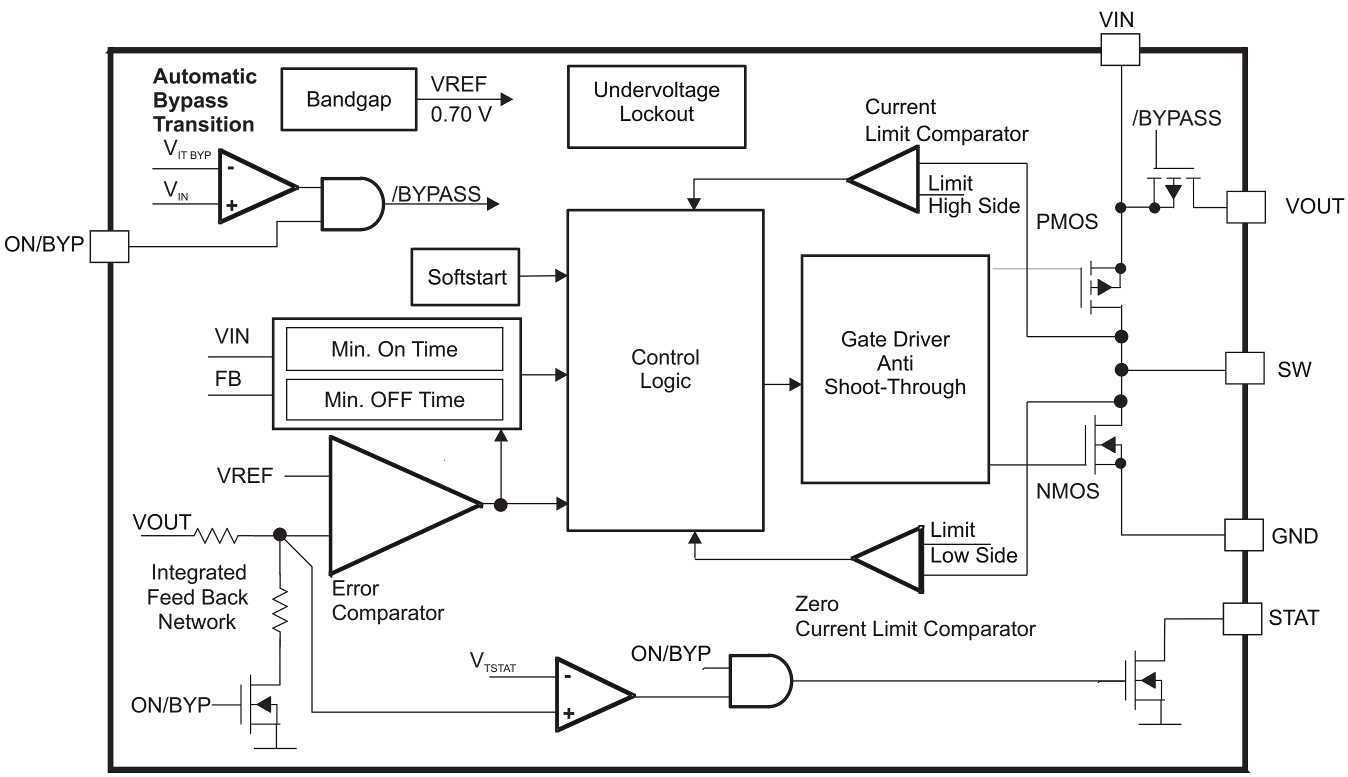
Figure 5. $r_{DS(ON)}$ NMOS vs Input Voltage

9 Detailed Description

9.1 Overview

The TPS62730 combines a synchronous buck converter for high efficient voltage conversion and an integrated ultra low power bypass switch to support low power modes of modern micro controllers and RF ICs.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 DCS-Control™

The TPS62730 includes TI's DCS-Control, an advanced regulation topology, that combines the advantages of hysteretic and voltage mode control architectures. While a comparator stage provides excellent load transient response, an additional voltage feedback loop ensures high DC accuracy as well. The DCS-Control enables switch frequencies up to 3 MHz, excellent transient and AC load regulation as well as operation with small and cost-competitive external components. The TPS6273x devices offer fixed output voltage options featuring smallest solution size by using only three external components. Furthermore this step-down converter provides excellent low output voltage ripple over the entire load range which makes this part ideal for RF applications. In the ultra low-power bypass mode, the output of the device VOUT is directly connected to the input VIN through the internal bypass switch. In this mode, the buck converter is shut down and consumes only 30 nA typical input current. Once the device is turned from ultra low-power bypass mode into buck converter operation for an RF transmission, all the internal circuits of the regulator are activated within a start up time t_{Start} of typical 50 µs. During this time the bypass switch is still turned on and maintains the output VOUT connected to the input VIN. Once the DC-DC converter is settled and ready to operate, the internal bypass switch is turned off and the system is supplied by the output capacitor and the other decoupling capacitors. The buck converter kicks in once the capacitors connected to VOUT are discharged to the level of the nominal buck converter output voltage. Once the output voltage falls below the threshold of the internal error comparator, a switch pulse is initiated, and the high side switch of the DC-DC converter is turned on. The high-side switch remains turned on until a minimum on time of t_{ONmin} expires and the output voltage trips the threshold of the error comparator or the inductor current reaches the high side switch current limit. Once the high side switch turns off, the low side switch

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Feature Description (continued)

rectifier is turned on and the inductor current ramps down until the high side switch turns on again or the inductor current reaches zero. The converter operates in the PFM (pulse frequency modulation) mode during light loads, which maintains high efficiency over a wide load current range. In PFM mode, the device starts to skip switch pulses and generates only single pulses with the on time t_{ONmin}. The PFM mode of TPS62730 is optimized for low output ripple voltage if small external components are used.

The on time t_{ONmin} can be estimated to:

$$t_{ONmin} = \frac{V_{OUT}}{V_{IN}} \times 260\text{ ns}$$

where

- t_{ONmin}: High side switch on time [ns]
- V_{IN}: Input voltage [V]
- V_{OUT}: Output voltage [V]
- (1)

Therefore, the peak inductor current in PFM mode is approximately:

$$I_{LPFMpeak} = \frac{(V_{IN} - V_{OUT})}{L} \times t_{ONmin}$$

where

- V_{IN}: Input voltage [V]
- V_{OUT}: Output voltage [V]
- L : Inductance [µH]
- $I_{LPFMpeak}$: PFM inductor peak current [mA] (2)

9.3.2 ON/BYP Mode Selection

The DC-DC converter is activated when ON/BYP is set high. For proper operation, the ON/BYP pin must be terminated and may not be left floating. This pin is controlled by the RF transceiver or micro controller for proper mode selection. Pulling the ON/BYP pin low activates the ultra low-power bypass mode with typical 30-nA current consumption. In this mode, the internal bypass switch is turned on and the output of the DC-DC converter is connected to the battery VIN. All other circuits like the entire internal-control circuitry, the High Side and Low Side MOSFETs of the DC-DC output stage are turned off as well the internal resistor feedback divider is disconnected. The ON/BYP must be controlled by a microcontroller for proper mode selection. In case of CC2540, connect this to the power down signal which is output on one of the P1.x ports (see CC2540 user guide).

9.3.3 STAT Open-Drain Output

The STAT output is active when the device is enabled (EN/BYP = high) and indicates the status of the output voltage. The STAT output is a open-drain output with active low level and needs a external pullup resistor to indicate a high level. It is driven by an internal comparator which monitors the output voltage V_{OUT}. The STAT pin is tied to low level, if the output voltage V_{OUT} is considered as valid and exceeding the threshold V_{TSTAT} (95% of V_{OUT} for falling V_{IN} and 98% of V_{OUT} for rising V_{IN}). The pin is high impedance with the ON/BYP pin set to low level or V_{OUT} is below the V_{TSTAT} threshold. If not used, the STAT pin can be left open. See Figure 6 and Figure 7.

Feature Description (continued)

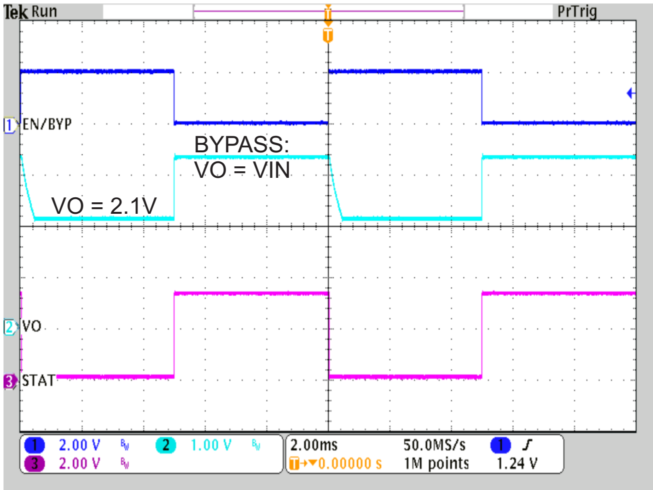

Figure 6. Operation Mode Transition ON/BYP = High/Low, R_{Load} = 1k

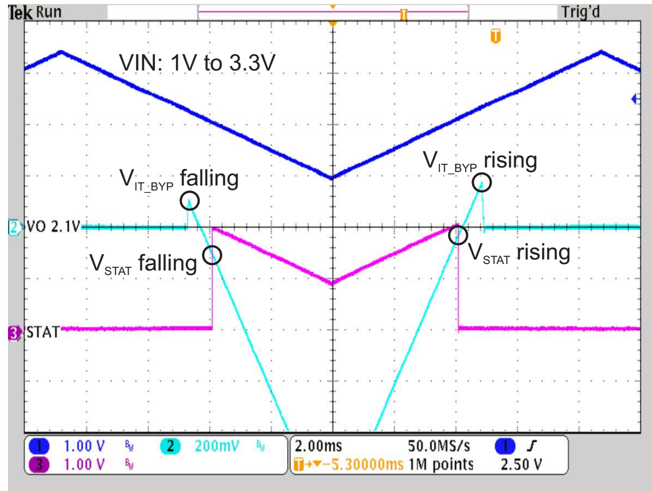

Figure 7. STAT Pin / VOUT Behavior With EN/BYP = High, R_{Load} = 1k

9.4 Device Functional Modes

9.4.1 Start-Up

Once the device is supplied with a battery voltage, the bypass switch is activated. If the ON/BYP pin is set to high, the device operates in bypass mode until the DC-DC converter has settled and can kick in. During start-up, high peak currents can flow over the bypass switch to charge up the output capacitor and the additional decoupling capacitors in the system.

9.4.2 Automatic Transition from DC-DC to Bypass Operation

With the ON/BYP pin set to high, the TPS62730 is active and features an automatic transition between DC-DC and bypass mode to reduce the output ripple voltage to zero. Once the input voltage comes close to the output voltage of the DC-DC converter, the DC-DC converters operates close to 100% duty cycle operation. At this operating condition, the switch frequency would start to drop and would lead to increased output ripple voltage. The internal bypass switch is turned on once the battery voltage at VIN trips the Automatic Bypass Transition Threshold VIT BYP for falling VIN. The DC-DC regulator is turned off and therefore it generates no output ripple voltage. Due to the output is connected through the bypass switch to the input, the output voltage follows the input voltage minus the voltage drop across the internal bypass switch. In this mode the current consumption of the DC-DC converter is reduced to typically 23 µA. Once the input voltage increases and trips the bypass deactivation threshold VIT BYP for rising VIN, the DC-DC regulator turns on and the bypass switch is turned off. See Figure 7 and Figure 24.

9.4.3 Internal Current Limit

The TPS62730 integrates a High Side and Low Side MOSFET current limit to protect the device against heavy load or short circuit when the DC-DC converter is active. The current in the switches is monitored by current limit comparators. When the current in the High Side MOSFET reaches its current limit, the High Side MOSFET is turned off and the Low Side MOSFET is turned on to ramp down the current in the inductor. The High Side MOSFET switch can only turn on again, once the current in the Low Side MOSFET switch has fallen below the threshold of its current limit comparator. The bypass switch does not feature a current limit to support lowest current consumption.

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS62730 is a high-frequency synchronous step down DC-DC converter optimized for ultra low-power wireless applications. The device is optimized to supply TI's Low-Power Wireless sub 1-GHz and 2.4-GHz RF transceivers and system-on-chip (SoC) solutions.

10.2 Typical Application

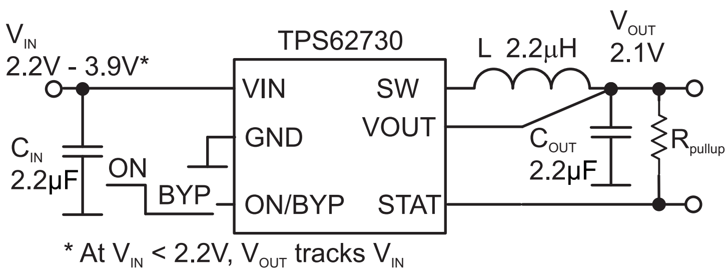

Figure 8. Typical Application

10.2.1 Design Requirements

The TPS6273x is a highly integrated DC-DC converter. The output voltage is internally fixed and does not require and external feedback divider network. For proper operation only a input- and output capacitor and an inductor is required. Table 1 shows the components used for the application characteristic curves.

Table 1. List of Components

REFERENCE	DESCRIPTION	VALUE	MANUFACTURER	DIMENSIONS
TPS62730	Step-down converter with bypass mode		Texas Instruments	1.5 x 1.0 x 0.55 mm
CIN, COUT	Ceramic capacitor 0402 X5R 6.3V GRM155R60J225	2.2 µF	Murata	1.0 x 0.5 x 0.5 mm
L	Inductor MIPSZ2012 2R2	2.2 µH	FDK	2.0 x 1.2 x 1.0 mm

10.2.2 Detailed Design Procedure

10.2.2.1 Output Filter Design (Inductor and Output Capacitor)

The TPS62730 is optimized to operate with effective inductance values in the range of 1.5 µH to 3 µH and with effective output capacitance in the range of 1.0 µF to 10 µF. The internal compensation is optimized to operate with an output filter of L = 2.2 µH and C_{OUT} = 2.2 µF, which gives and LC output filter corner frequency of:

$$f_C = \frac{1}{2 \times \pi \times \sqrt{(2.2\mu H \times 2.2\mu F)}} = 72kHz \tag{3}$$

10.2.2.2 Inductor Selection

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor must be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT}. Equation 4 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 5.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f}$$

where

- f = Switching Frequency
- L = Inductor Value
- ΔI_L= Peak-to-Peak inductor ripple current (4)

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2}$$

where

- ΔI_L= Peak-to-Peak inductor ripple current
- I_{Lmax} = Maximum Inductor current (5)

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (that is, quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance, $R_{(DC)}$, and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS62730 converters.

Table 2. List of Inductors

INDUCTANCE [µH]	DIMENSIONS [mm3]	INDUCTOR TYPE	SUPPLIER
2.2	2.0 × 1.2 × 1.0	LQM21PN2R2NGC	Murata
2.2	2.0 × 1.2 × 1.0	MIPSZ2012	FDK

10.2.2.3 DC-DC Output Capacitor Selection

The DCS-Control scheme of the TPS62730 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. At light load currents the converter operate in power save mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current.

10.2.2.4 Additional Decoupling Capacitors

In addition to the output capacitor there are further decoupling capacitors connected to the output of the TPS62730. These decoupling capacitor are placed closely at the RF transmitter or micro controller. The total capacitance of these decoupling capacitors should be kept to a minimum and should not exceed the values given in the reference designs, see Figure 31 and Figure 32. During mode transition from DC-DC operation to bypass mode the capacitors on the output VOUT are charged up to the battery voltage VIN through the internal bypass

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switch. During mode transition from bypass mode to DC-DC operation, these capacitors must be discharged by the system supply current to the nominal output voltage threshold until the DC-DC converter will kick in. The charge change in the output and decoupling capacitors can be calculated according to Equation 6. The energy loss due to charge and discharge of the output and decoupling capacitors can be calculated according to Equation 7.

$$dQ_{COUT\_CDEC} = C_{COUT\_CDEC} \times \left(V_{IN} - V_{OUT\_DC\_DC}\right)$$

where

- dQ_{COUT_CDEC} : Charge change needed to charge up and discharge the output and decoupling capacitors from VOUT_DC_DC to V_{IN} and vice versa
- C_{COUT_CDEC}: Total capacitance on the VOUT pin of the device, includes output and decoupling capacitors
- V_{IN}: Input (battery) voltage
- $V_{OUT\_DC\_DC}$: nominal DC-DC output voltage V_{OUT} (6)

$$E_{Charge\_Loss} = \frac{1}{2} \times C_{COUT\_CDEC} \times \left(V_{IN}^{2} - V_{OUT\_DC\_DC}^{2}\right)$$

where

- C_{COUT_CDEC}: Total capacitance on the VOUT pin of the device, includes output and decoupling capacitors
- V_{IN}: Input (battery) voltage
- $V_{OUT\_DC\_DC}$: nominal DC-DC output voltage V_{OUT} (7)

10.2.2.5 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering to ensure proper function of the device and to minimize input voltage spikes. For most applications a 2.2 µF to 4.7 µF ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input voltage filtering.

Table 3 shows a list of tested input/output capacitors.

10.2.2.5.1 Input Buffer Capacitor Selection

In addition to the small ceramic input capacitor a larger buffer capacitor C_{Buf} is recommended to reduce voltage drops and ripple voltage. When using battery chemistries like Li-SOCl2, Li-SO2, Li-MnO2, the impedance of the battery must be considered. These battery types tend to increase their impedance depending on discharge status and often can support output currents of only a few mA. Therefore a buffer capacitor is recommended to stabilize the battery voltage during DC-DC operations (for example, for an RF transmission). A voltage drop on the input of the TPS62730 during DC-DC operation impacts the advantage of the step-down conversion for system power reduction. Furthermore the voltage drops can fall below the minimum recommended operating voltage of the device and leads to an early system cut off. Both impacts effects reduce the battery life time. To achieve best performance and to extract most energy out of the battery, a good procedure is to design the select the buffer capacitor value for an voltage drop below 50 mVpp during DC-DC operation. The capacitor value strongly depends on the used battery type, as well the current consumption during an RF transmission as well the duration of the transmission.

Table 3. List of Capacitor

CAPACITANCE [µF]	SIZE	CAPACITOR TYPE	SUPPLIER
2.2	0402	GRM155R60J225	Murata

10.2.2.6 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

Basic signals must be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the High Side MOSFET, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta I_{(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (for example, MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis must be done over the input voltage range, load current range, and temperature range.

10.2.3 Application Curves

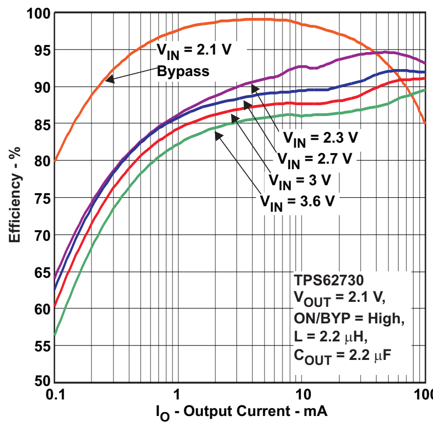

Figure 9. Efficiency vs Output Current

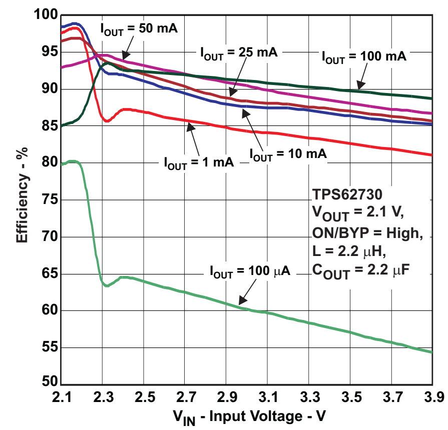

Figure 10. Efficiency vs Input Voltage

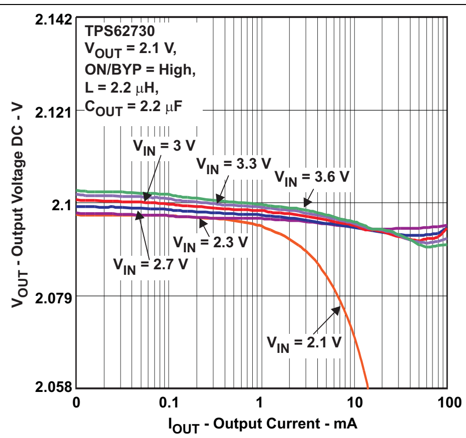

Figure 11. Output Voltage vs Output Current

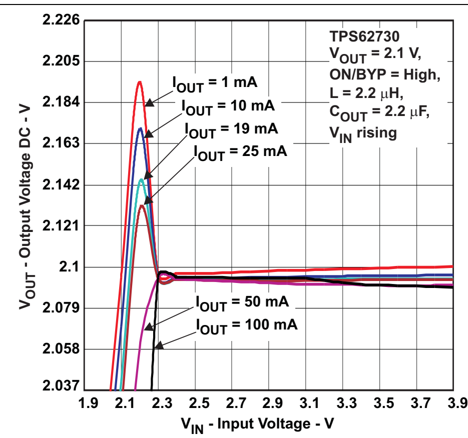

Figure 12. Output Voltage vs Input Voltage

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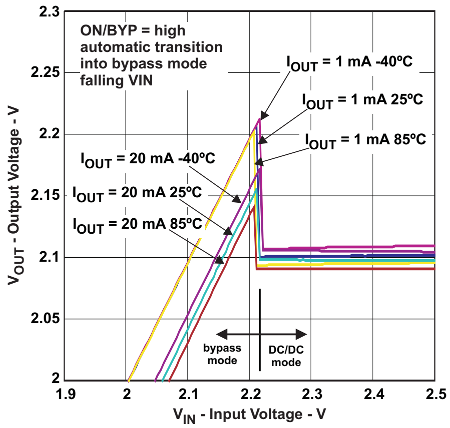

Figure 13. Automatic Transition into Bypass Mode - Falling V_{IN}

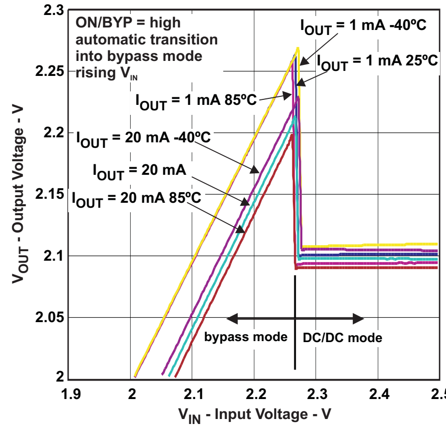

Figure 14. Automatic Transition into Bypass Mode - Rising V_{IN}

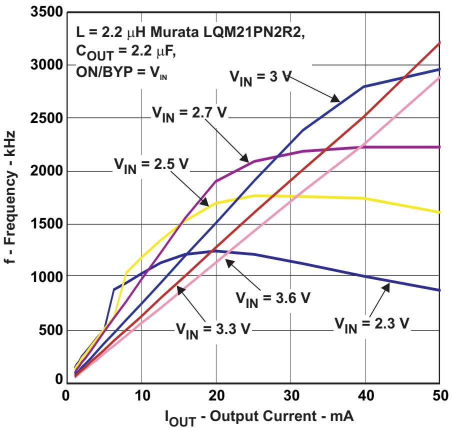

Figure 15. Switching Frequency vs I_{OUT} vs V_{IN}

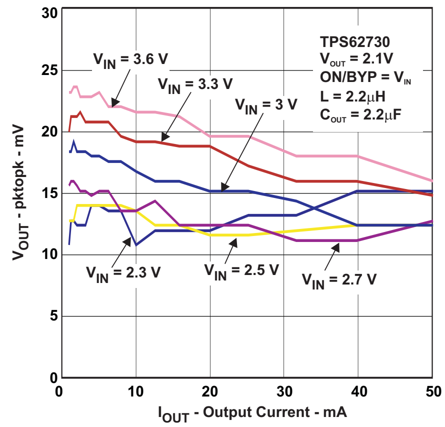

Figure 16. V_{OUT} vs I_{OUT} vs V_{IN}

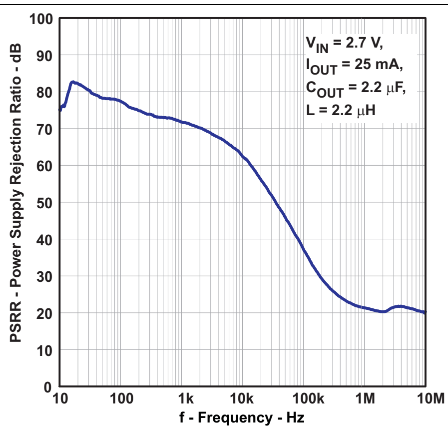

Figure 17. PSRR vs Frequency

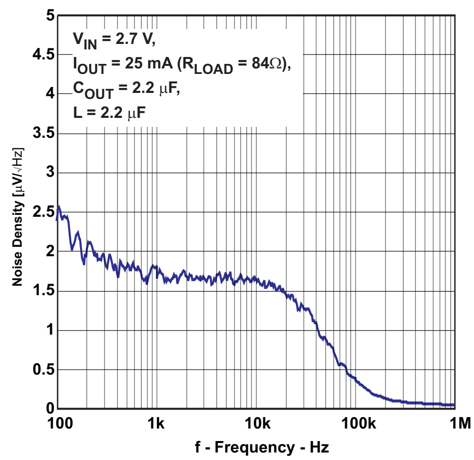

Figure 18. Noise Density vs Frequency

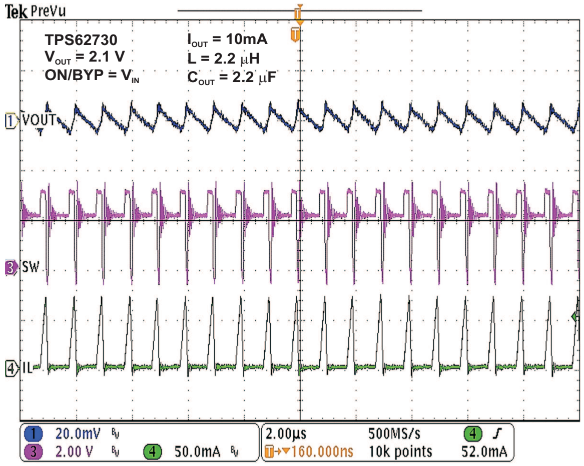

Figure 19. DC-DC Mode Operation I_{OUT} = 10 mA

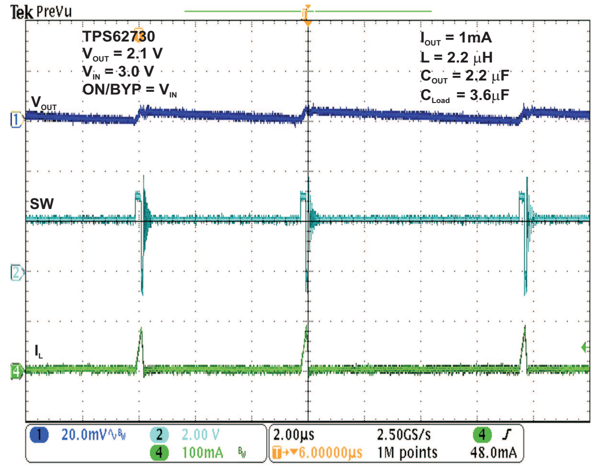

Figure 20. DC-DC Mode Operation I_{OUT} = 1 mA

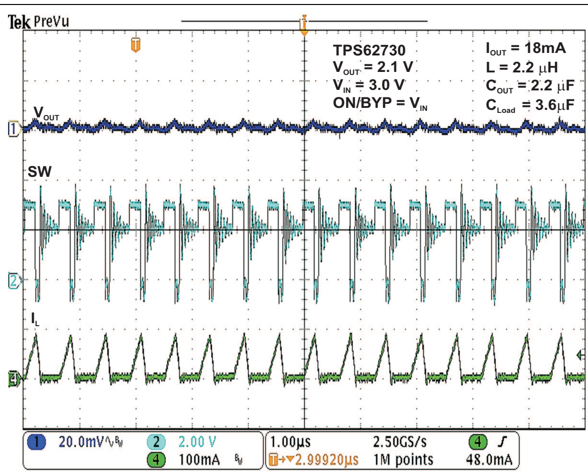

Figure 21. DC-DC Mode Operation I_{OUT} = 18 mA

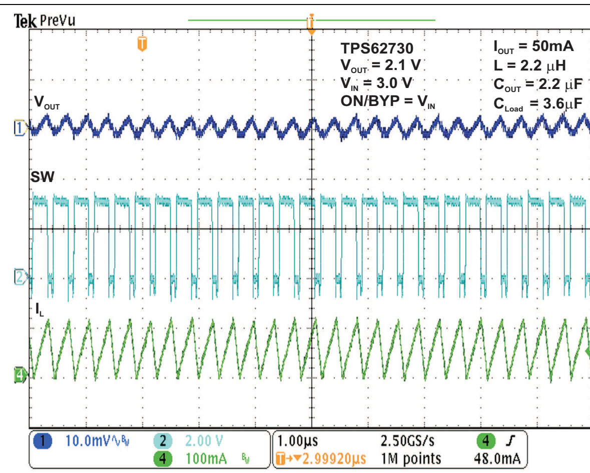

Figure 22. DC-DC Mode Operation I_{OUT} = 50 mA

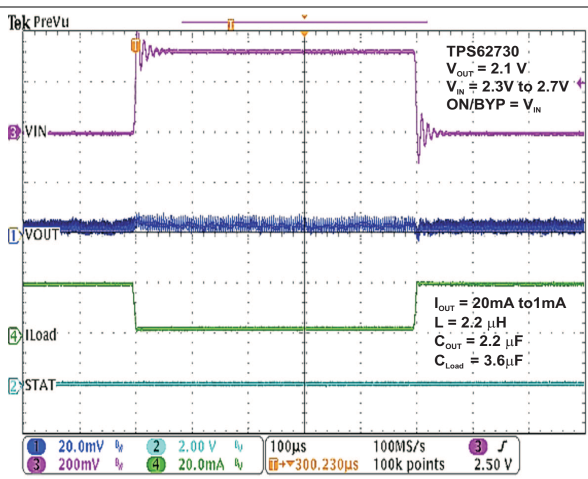

Figure 23. DC-DC Mode Operation Line and Load Transient Performance

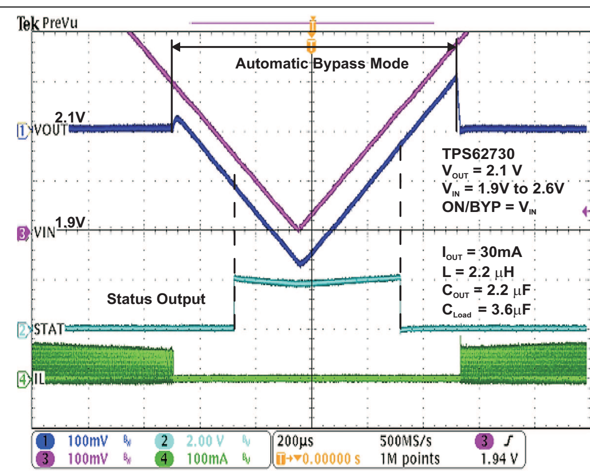

Figure 24. Automatic Bypass Transition with Falling / Rising Input Voltage V_{IN}

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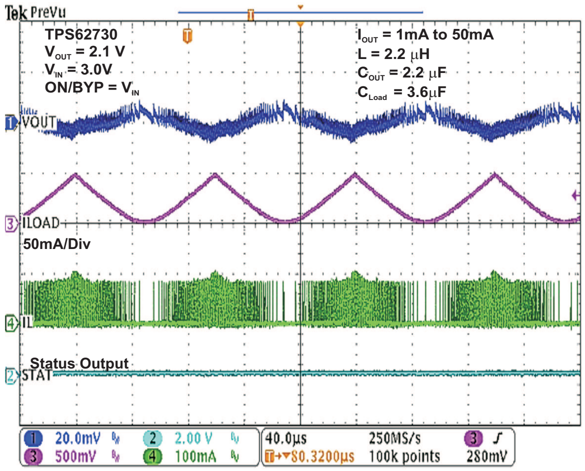

Figure 25. DC-DC Mode V_{OUT} AC Load Regulation Performance

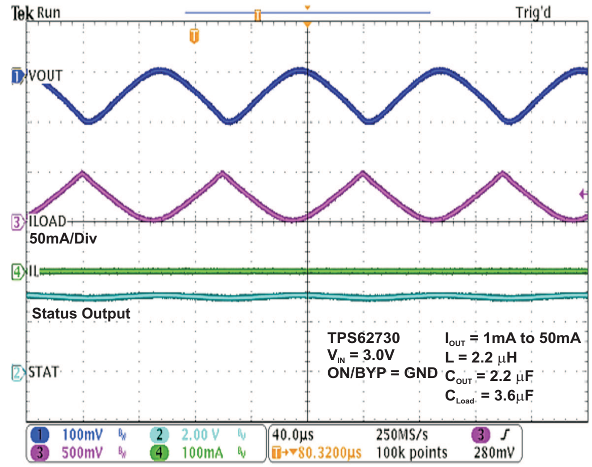

Figure 26. Bypass Mode Operation V_{OUT} AC Behavior ON/BYP = GND

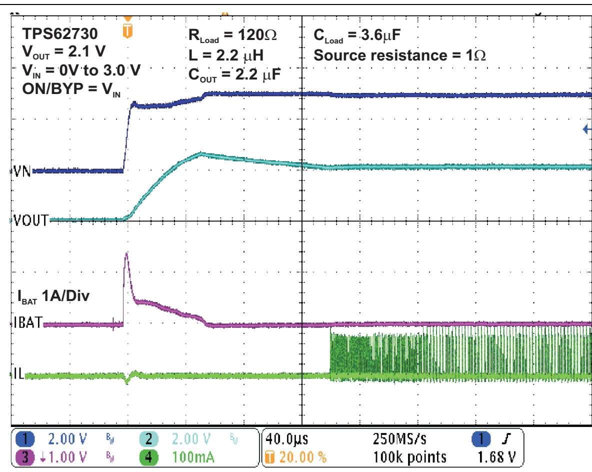

Figure 27. Start-Up Behavior

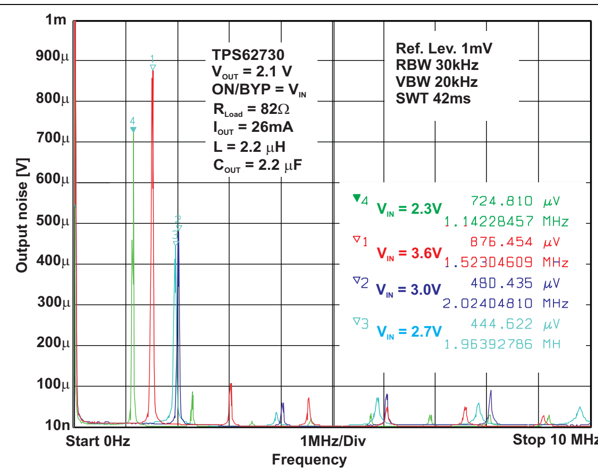

Figure 28. Spurious Output Noise TPS62730 I_{OUT} 26 mA

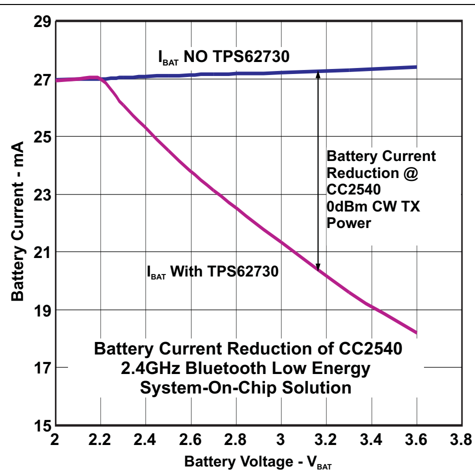

Figure 29. Battery Current Reduction vs Battery Voltage

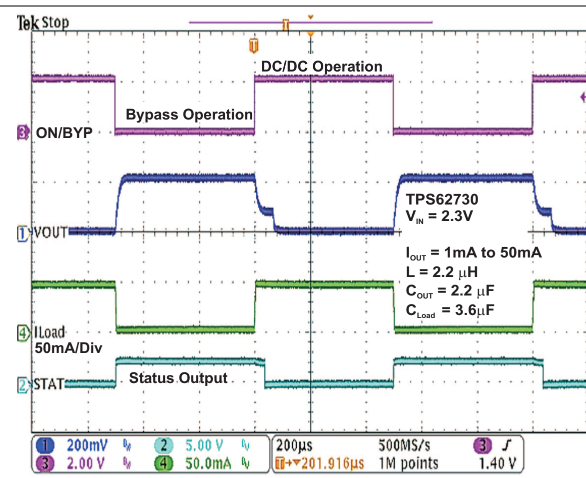

Figure 30. Mode Transition ON/BYP Behavior

10.3 System Examples

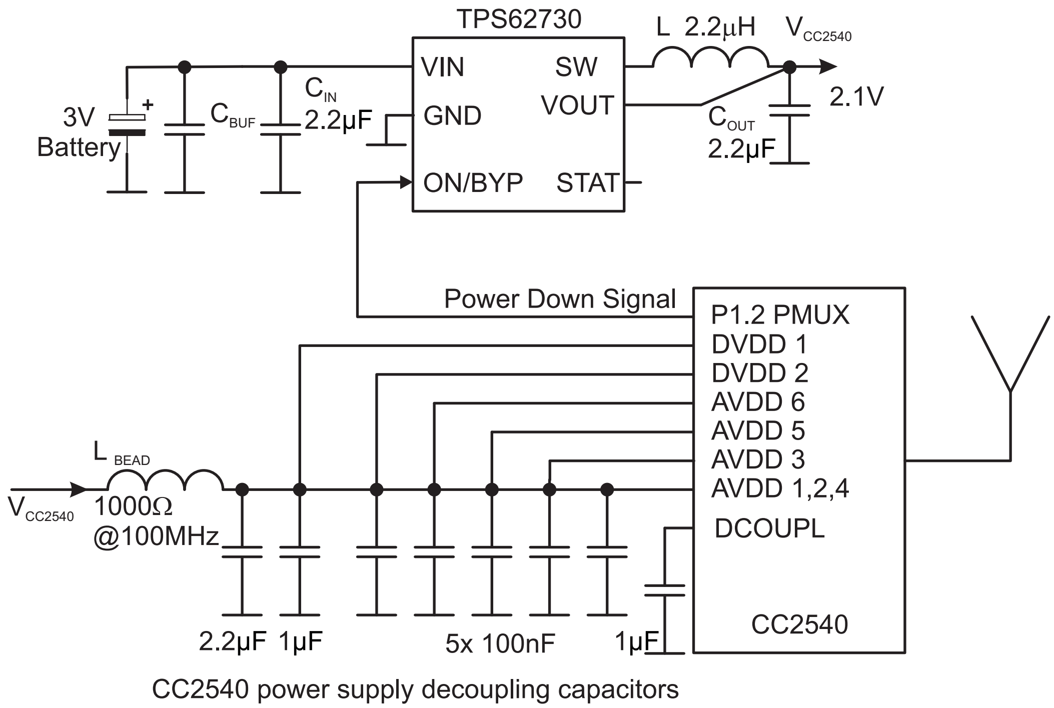

Figure 31. System Example CC2540

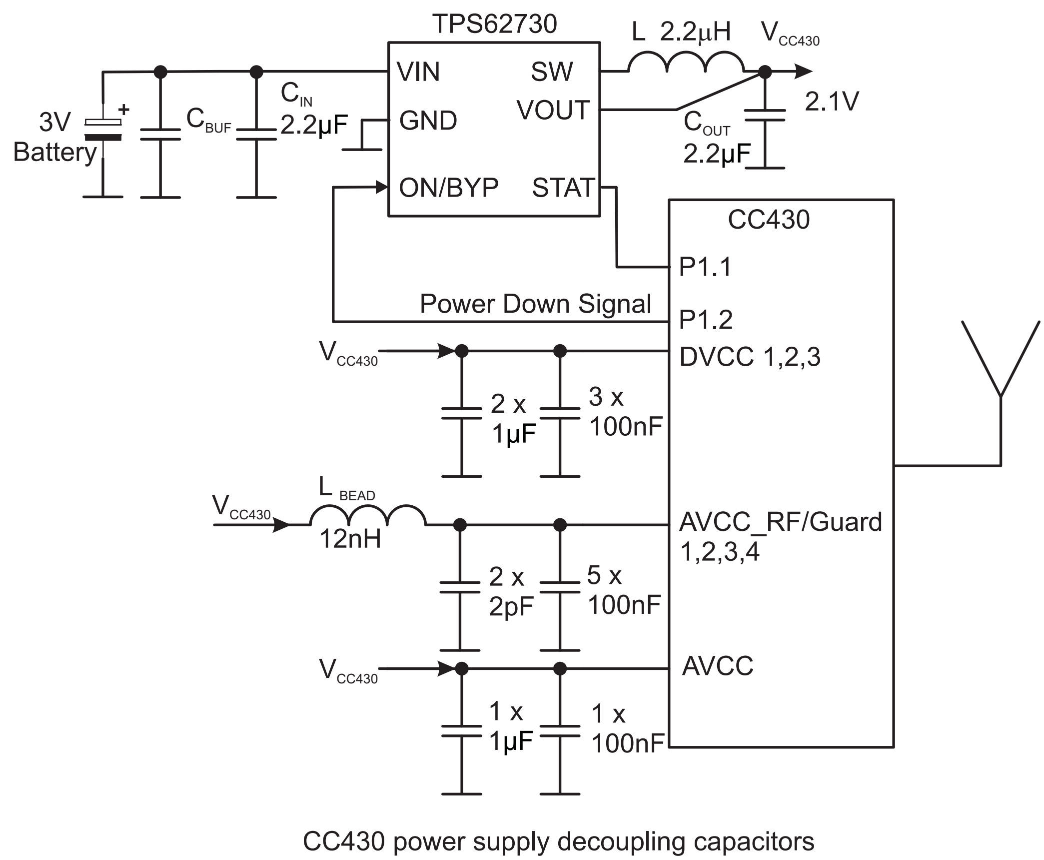

Figure 32. System Example CC430

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11 Power Supply Recommendations

The power supply to the TPS62730 must have a current rating according to the supply voltage, output voltage and output current of the TPS62730.

12 Layout

12.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Especially RF designs demand careful attention to the PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems and interference with RF circuits. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. Use a common Power GND node and a different node for the Signal GND to minimize the effects of ground noise. Keep the common path to the GND PIN, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. The VOUT line should be connected to the output capacitor and routed away from noisy components and traces (for example, SW line).

12.2 Layout Example

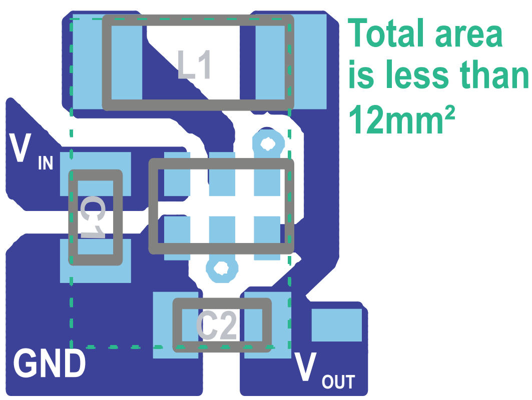

Figure 33. Recommended PCB Layout for TPS62730

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62730	Click here	Click here	Click here	Click here	Click here
TPS62732	Click here	Click here	Click here	Click here	Click here
TPS62733	Click here	Click here	Click here	Click here	Click here

13.3 Trademarks

Bluetooth is a trademark of Bluetooth SIG.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62730DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RP	Samples
TPS62730DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RP	Samples
TPS62732DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RR	Samples
TPS62732DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RR	Samples
TPS62733DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA	Samples
TPS62733DRYT	ACTIVE	SON	DRY	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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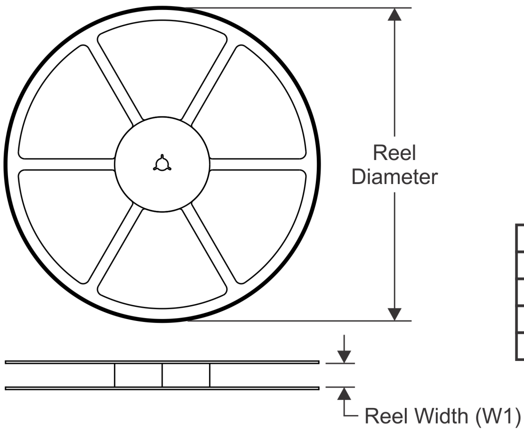
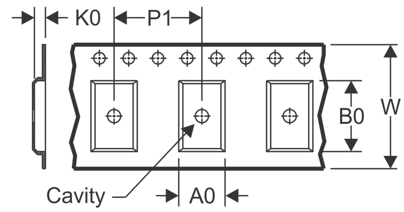
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

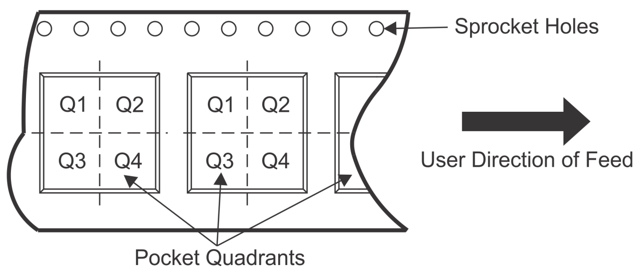


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

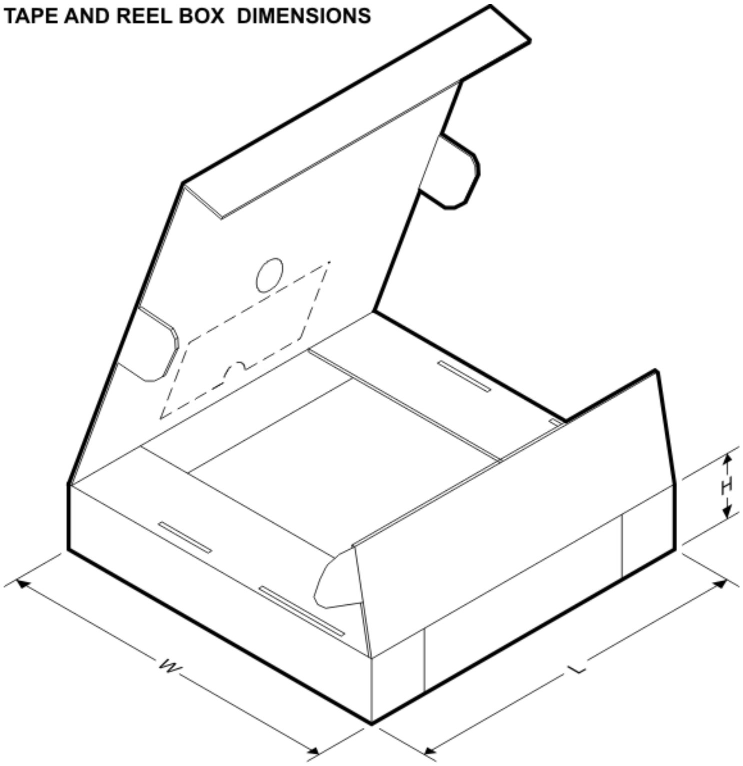
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62730DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS62730DRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS62732DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS62732DRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS62733DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS62733DRYT	SON	DRY	6	250	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1

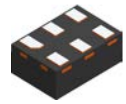
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62730DRYR	SON	DRY	6	5000	200.0	183.0	25.0
TPS62730DRYT	SON	DRY	6	250	200.0	183.0	25.0
TPS62732DRYR	SON	DRY	6	5000	200.0	183.0	25.0
TPS62732DRYT	SON	DRY	6	250	203.0	203.0	35.0
TPS62733DRYR	SON	DRY	6	5000	200.0	183.0	25.0
TPS62733DRYT	SON	DRY	6	250	200.0	183.0	25.0

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

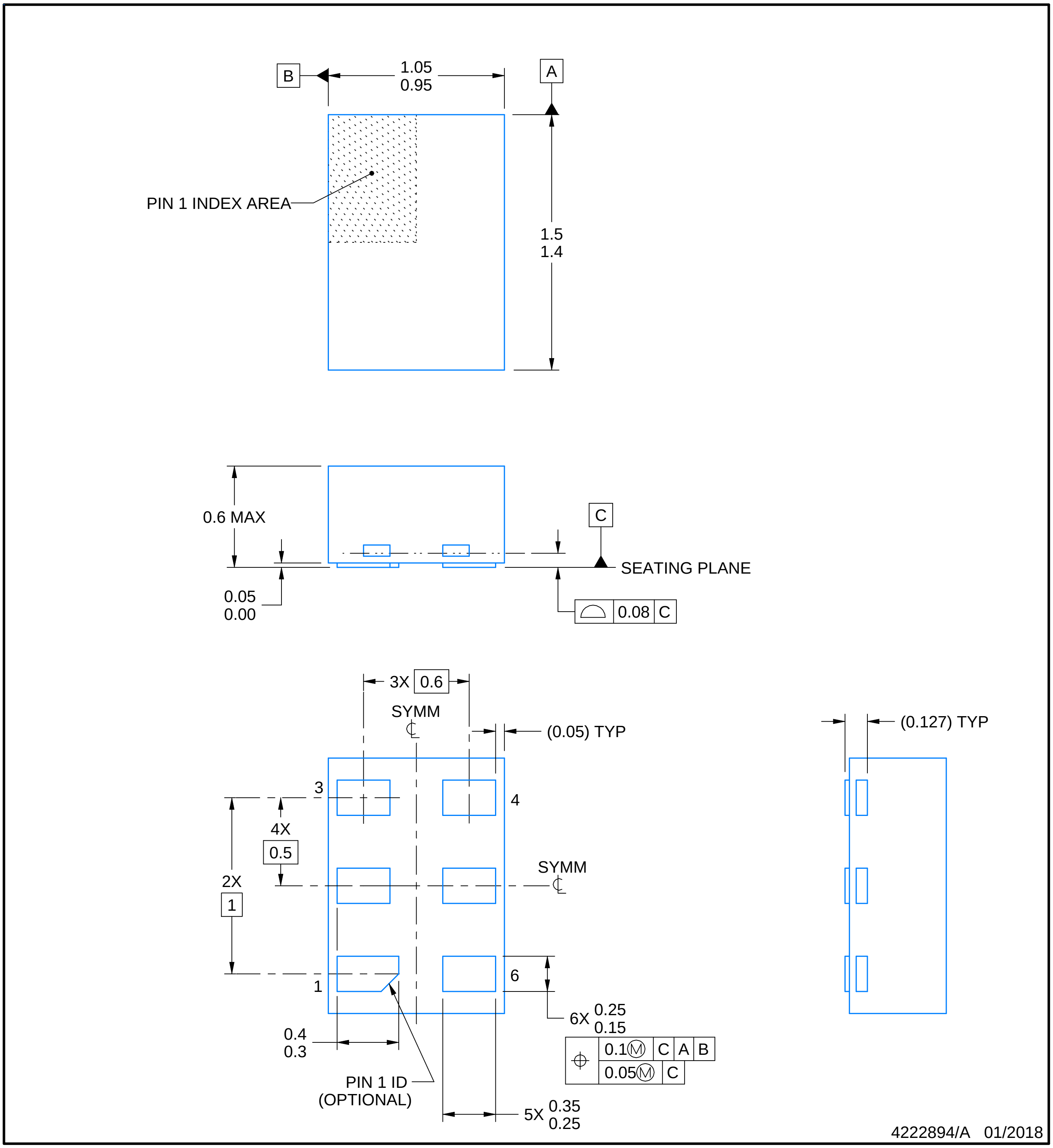


PACKAGE OUTLINE

DRY0006A

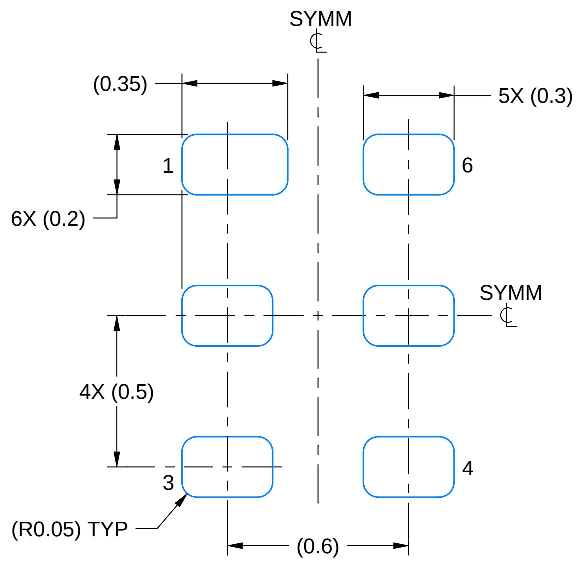
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

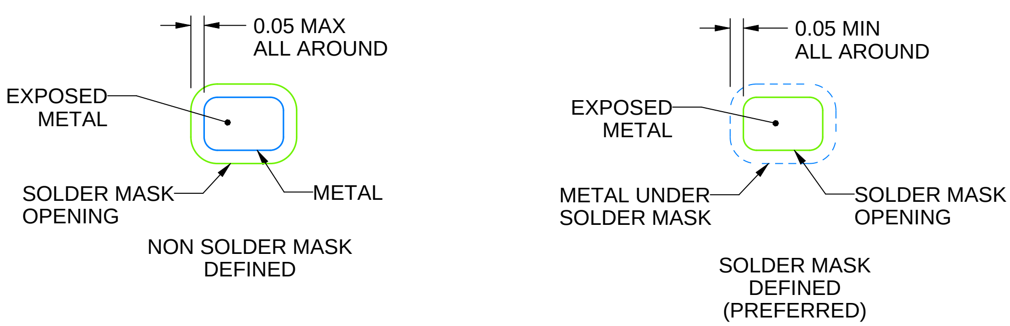


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

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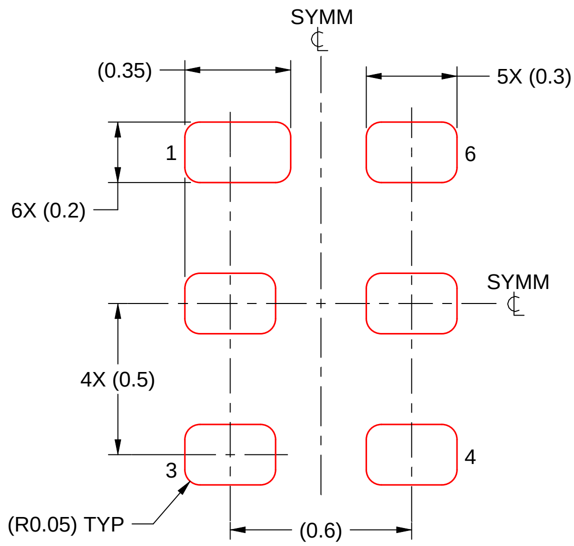
NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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